Digital to Analog Converter

Analog to Digital Converter

DAC - ADC

Digital to Analog Converter

- Function: converts binary input number in analog output;

$$f_{DAC}:N\rightarrow \mathbf{R}$$

- Parameters:
  - Conversion type: unipolar, bipolar;
  - Binary code (offset binary, two's complement, etc.);
  - Output type (U, I);
  - Output range $\Delta U = U_{O\_\max} - U_{O\_\min}$ $\Delta I = I_{O\_\max} - I_{O\_\min}$
  - Resolution - output variation for LSB variation of input code

    $$\delta U = U_{LSB} = \Delta U / (2^n - 1)$$

    - number of bits used for binary cod *(n)*
  - Settling time - interval between an input command and the time when the output reaches its final value;

- Binary representation (positive fixed point) of numbers (n_1+n_2+1 bits): $N=\sum_{k=-n_1}^{n_2} b_k 2^k \quad ; \quad b_k \in \{0,1\};$
- **Binary coding** (sub-unitary, N<1)
  - Natural binary (unsigned)

$$N=\sum_{k=1}^{n} b_k 2^{-k} \quad N_{\min}=0 \quad N_{\max}=1-2^{-n} \quad \delta N=2^{-n}$$

  - Offset binary (signed)

$$N=\sum_{k=1}^{n} b_k 2^{-k}-2^{-1} \quad N_{\min}=-\frac{1}{2} \quad N_{\max}=\frac{1}{2}-2^{-n} \quad \delta N=2^{-n}$$

  - Two's complement (signed)

$$N=\left(-2^{-1}\right)\cdot b_1+\sum_{k=2}^{n} b_k 2^{-k} \quad N_{\min}=-\frac{1}{2} \quad N_{\max}=\frac{1}{2}-2^{-n} \quad \delta N=2^{-n}$$

- **Binary coding** (cont'd)
  - Sign – Magnitude (signed)

$$N=(-1)^{b_1}\cdot\sum_{k=2}^{n}b_k 2^{-k} \quad N_{\min}=-2^{-1}+2^{-n} \quad N_{\max}=2^{+1}-2^{-n} \quad \delta N=2^{-n}$$

  - Binary coded decimal (BCD) – 4 bits (nibble) used to represent one digit ;
  - Gray – the difference between codes of two successive number is 1 bit;
  - One's complement (signed);

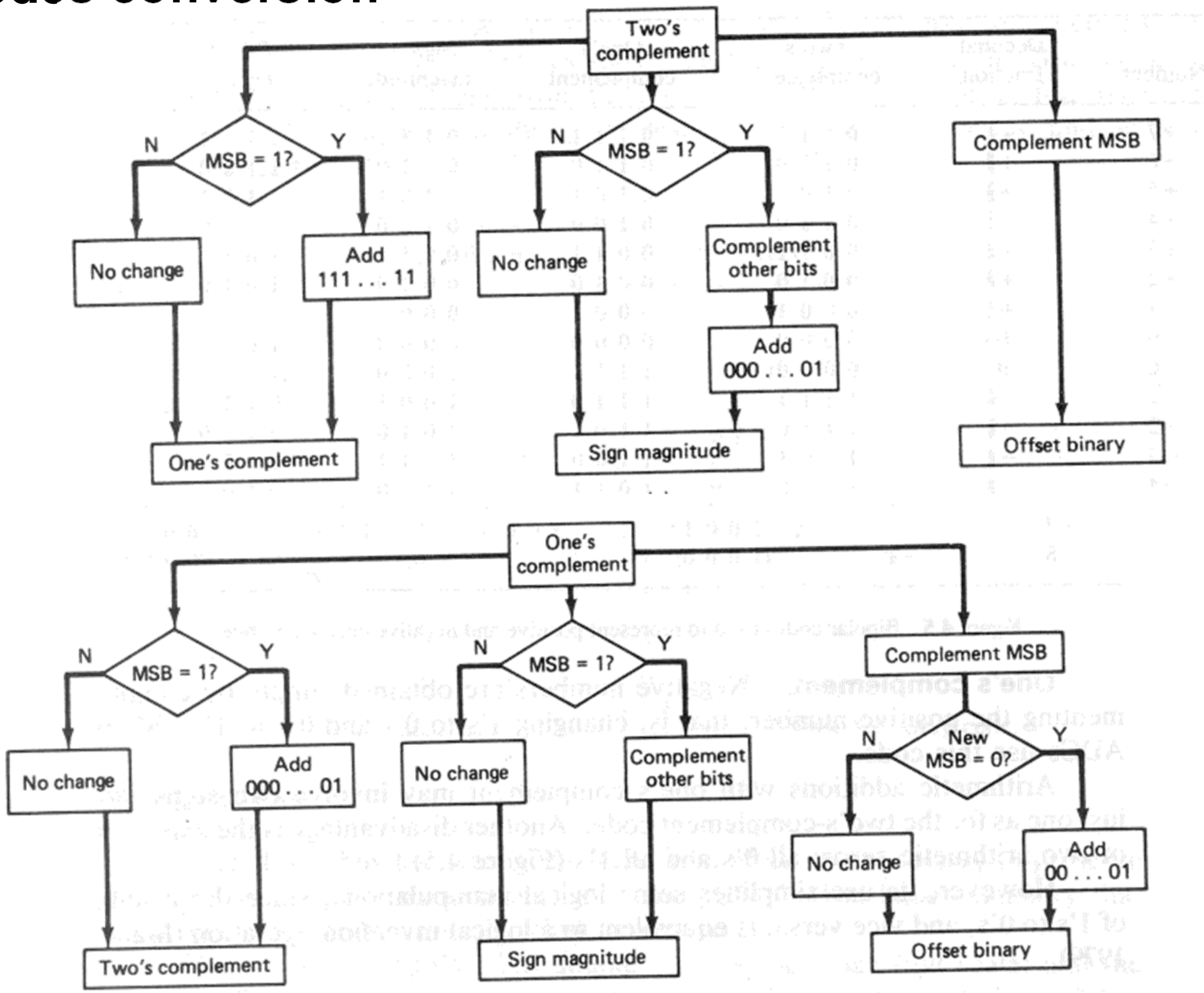
Unipolar Codes

N (natural)	Fraction (subunitar nr)	NB	BCD	Gray
0	0	0000	0000	0000
1	1/16	0001	0001	0001
2	2/16	0010	0010	0011
3	3/16	0011	0011	0010
4	4/16	0100	0100	0110
5	5/16	0101	0101	0111
6	6/16	0110	0110	0101
7	7/16	0111	0111	0100
8	8/16	1000	1000	1100
9	9/16	1001	1001	1101
10	10/16	1010	-	1111
11	11/16	1011	-	1110
12	12/16	1100	-	1010
13	13/16	1101	-	1011
14	14/16	1110	-	1001
15	15/16	1111	-	1000

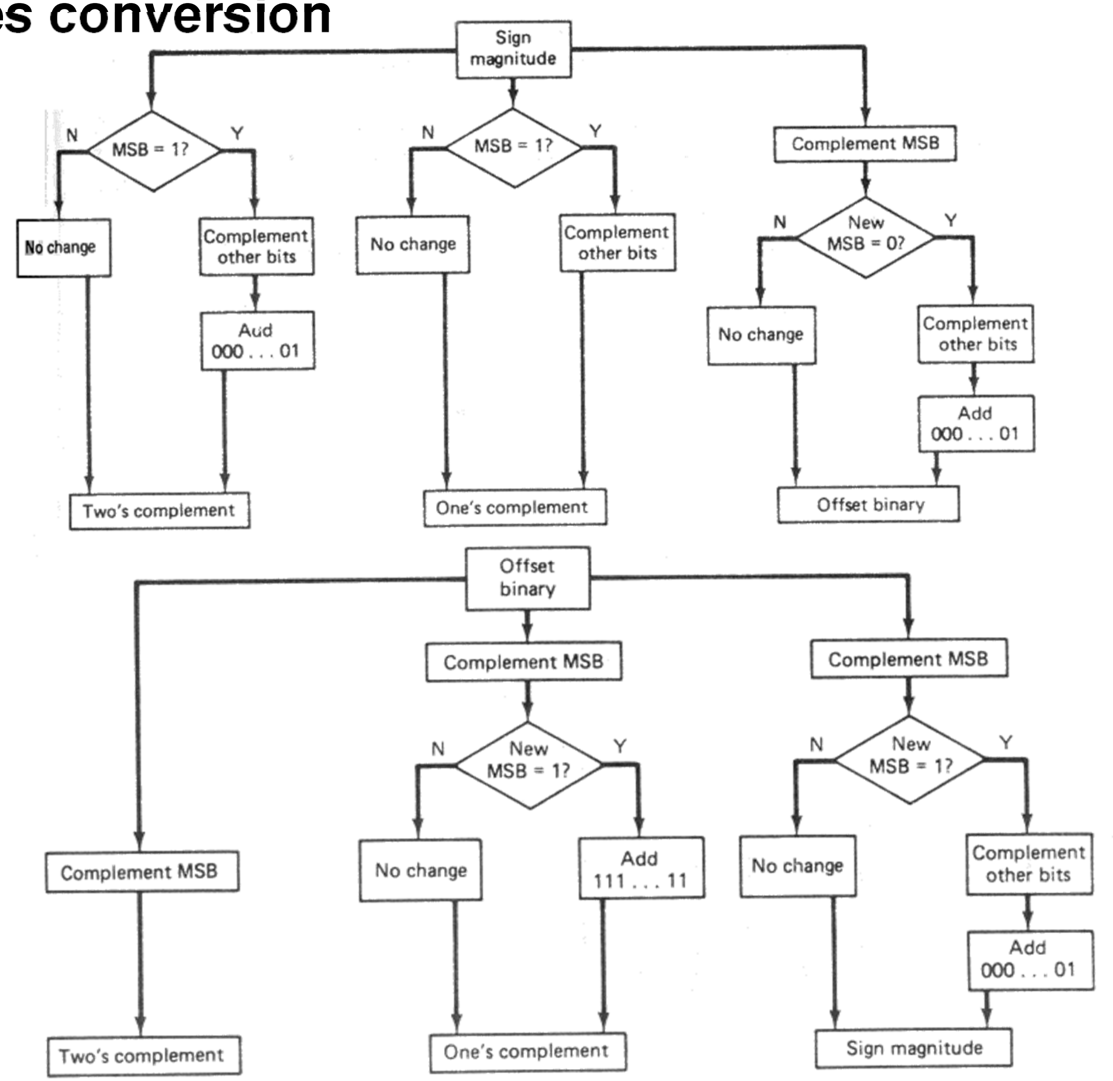
Bipolar Codes

N	Fraction	SM	C1	C2	OB*	OB
+3	+3/8	011	011	011	111	000
+2	+2/8	010	010	010	110	001
+1	+1/8	001	001	001	101	010
+0	+0	000	000	000	100	011
-0	-0	100	111	-	-	-
-1	-1/8	101	101	111	011	100
-2	-2/8	110	101	110	010	101
-3	-3/8	111	100	101	001	110
-4	-4/8	-	-	100	000	111

Binary codes conversion



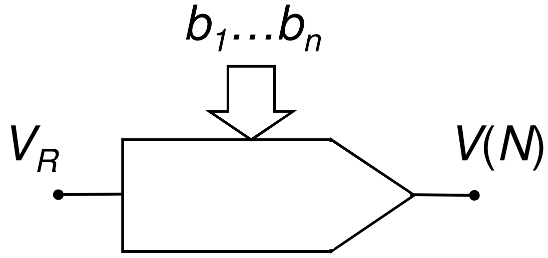
Binary codes conversion



(d)

- **Ideal characteristic for unipolar DAC :**

$$U(N) = U_R \cdot \sum_{k=1}^{n} b_k 2^{-k} \qquad \delta U = U_R \cdot 2^{-n} = \frac{U_{CS}}{2^n - 1}$$



$$U_{min} = U(N = 0..0\text{h}) = 0\text{V}$$

$$U_{max} = U(N = F...F\text{h}) = U_R\left(1 - 2^{-n}\right) = U_{CS}$$

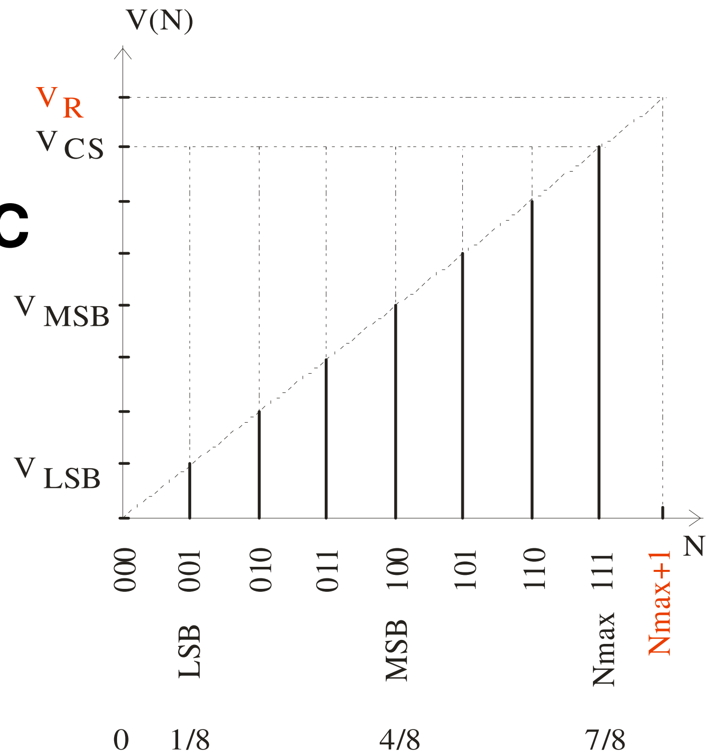
- **Ideal characteristic for bipolar DAC**

(offset binary code)

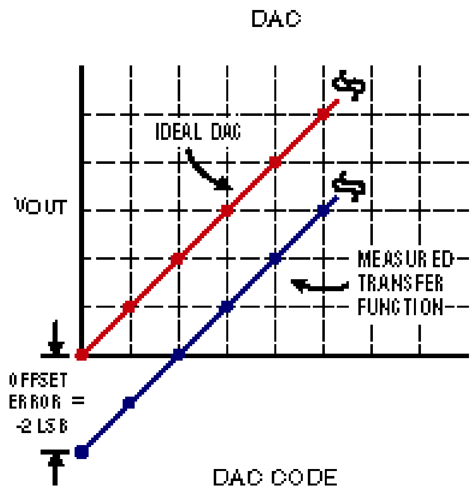
$$U(N) = U_R \cdot \left(\sum_{k=1}^{n} b_k 2^{-k} - 2^{-1} \right)$$

$$U_{min} = -U_R \cdot 2^{-1} \qquad U_{max} = U_R \cdot \left(2^{-1} - 2^{-n}\right)$$

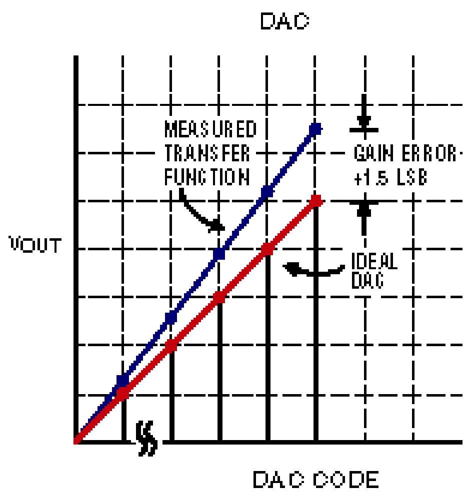
$$\delta U = U_R \cdot 2^{-n}$$



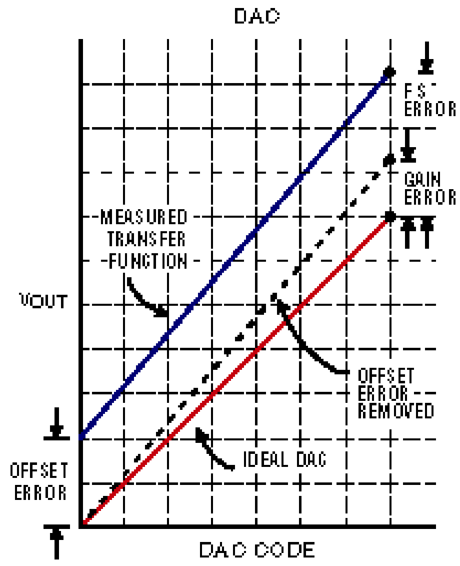
- **Non-ideality errors**
  - **Static errors**
    - Offset error – analog output response to an input code corresponding to output zero;
    - Gain error – difference between slope of actual and ideal transfer function;
    - Full-Scale error - difference between the actual and the ideal output maximum value (offset error + gain error) ;
    - Integrated nonlinearity error (INL) - deviation of an actual transfer function from a straight line (after nullifying offset and gain errors);
    - Differential nonlinearity error (DNL) - difference between the ideal and the measured output responses for successive DAC codes;
  - **Dynamic error**: overshoot, undershoot (during settling time)



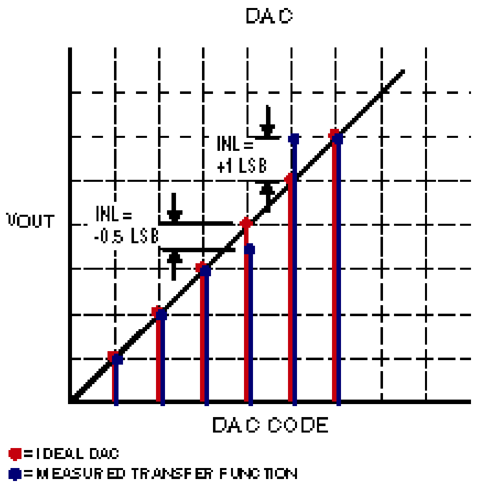
Offset error



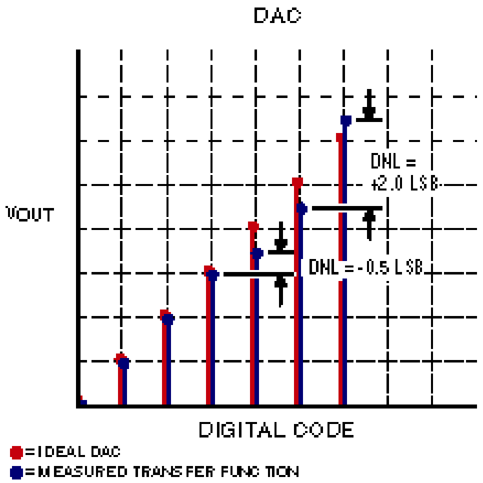
Gain error



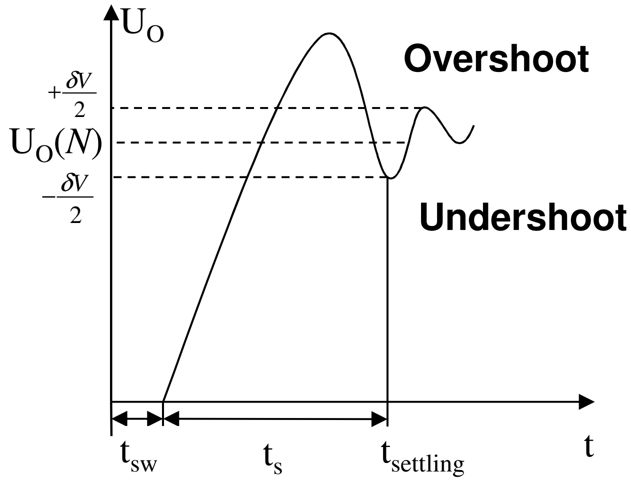
Factor scale error



INL error

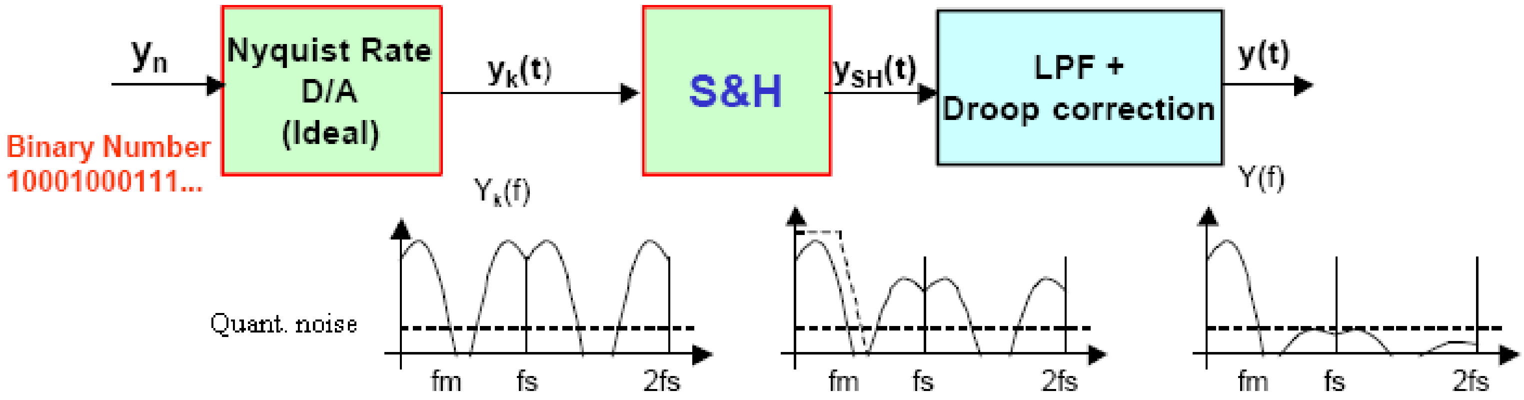


DNL error



Settling time

D/A converter – traditional data converter at Nyquist rate ($f_s > 2f_m$)



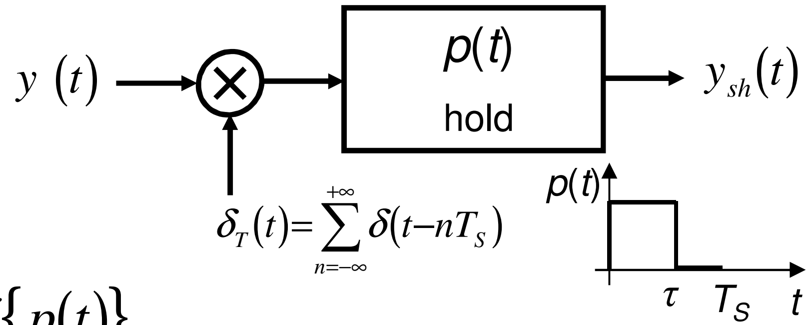
- LPF is antialiasing filter (for extinction of image signal on f_S) ;

- Droop correction means inverse “Sinc” function ;
- The S/H is a “deglitching” circuit and could be eliminated for small glitches;

D/A converter – mathematical representation:

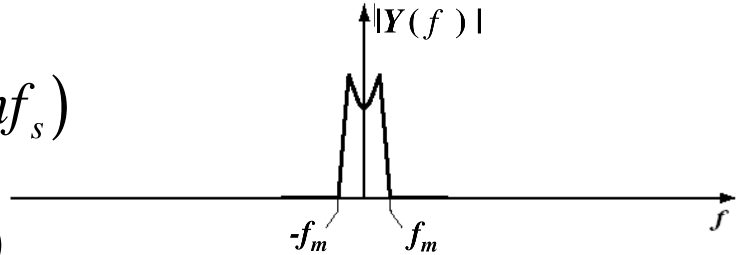
Pulse Amplitude Modulation

$$y_{sh}(t)=\left\{\sum_{n=-\infty}^{+\infty} y(t)\cdot\delta(t-nT_S)\right\}\otimes p(t)$$



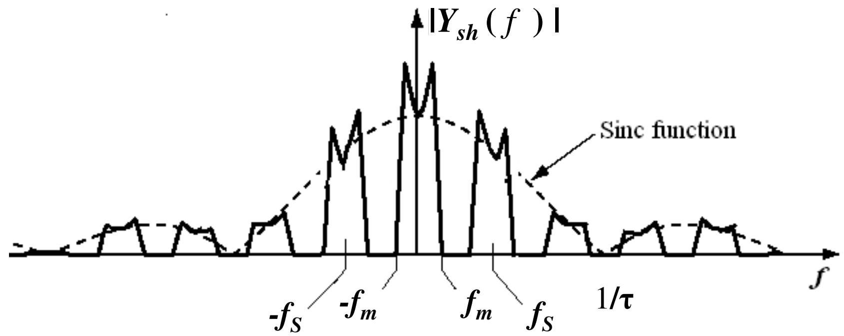
$$\mathcal{F}\{y_{sh}(t)\}=\mathcal{F}\left\{\sum_{n=-\infty}^{+\infty} y(nT_S)\cdot\delta(t-nT_S)\right\}\cdot\mathcal{F}\{p(t)\}$$

$$Y_{sh}(f)=\frac{\tau}{T_S}\cdot e^{-j\pi f\tau}\operatorname{sinc}(\pi f\cdot\tau)\sum_{n=-\infty}^{\infty}Y_k(f-nf_s)$$



For $w = T_S$ (practical DAC converter)

$$Y_{sh}(f)=\operatorname{sinc}\left(2\pi f\cdot\frac{T_s}{2}\right)\cdot\sum_{n=-\infty}^{\infty}Y_k(f-nf_s)$$



Types of DAC's

- Binary Weighted Resistor Network
- R-2R Ladder Network
- Stochastic
- Multiplying DAC

Binary-Weighted Resistor DAC

Using Tellegen's theorem:

$$V_g(N)\cdot\left(\sum_{i=1}^{n}\frac{1}{2^i R}+\frac{1}{2^n R}\right)=V_R\sum_{i=1}^{n}\frac{b_i}{2^i R}\qquad b_i\in\{0,1\}$$

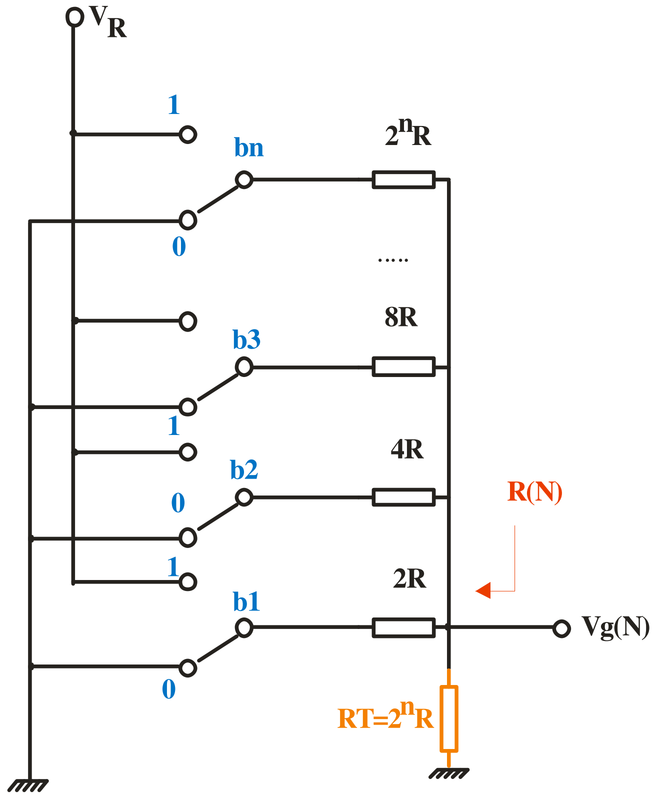
$$V_g(N)=V_R\sum_{i=1}^{n}b_i 2^{-i}=V_R\cdot N$$

$$V_{g\_min}=V_g(0\ldots 0\mathrm{h})=0\mathrm{V}\qquad \delta V_g=V_g(0\ldots 1\mathrm{h})=2^{-n}\,\mathrm{V_R}$$

$$V_{g\_max}=V_g(F\ldots F\mathrm{h})=V_R\left(1-2^{-n}\right)$$

After source passivization:

$$\frac{1}{R(N)}=\sum_{i=1}^{n}\frac{1}{2^i R}+\frac{1}{2^n R}=\frac{1}{R}\;\Rightarrow\;R(N)=R$$



Binary-Weighted Resistor DAC (cont'd)

Steady state voltage command

$$V_0(N)=V_g(N)$$

Dynamic regime (Laplace transform)

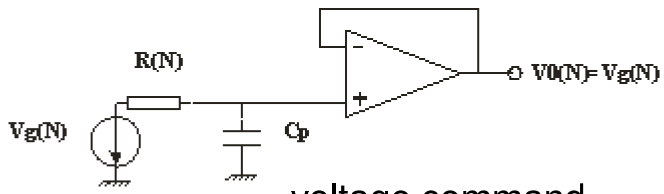
$$V_0(s)=V_g(s)\cdot\frac{1}{sRC_p+1}\cdot\frac{1}{s}=V_g(s)\cdot\left(\frac{1}{s}-\frac{1}{s+1/\tau}\right)$$

$$V_0(t)=V_g\cdot\left(1-e^{-\frac{t}{\tau}}\right)\cdot\sigma(t)\,,\qquad \tau=\frac{1}{R(N)C_p}$$

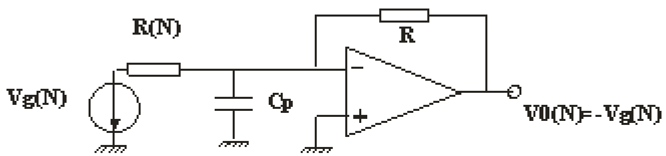
$$\left|V_0(t_s)-V_g(N)\right|\le\frac{1}{2}\delta V\;\Rightarrow\; t_s\ge\tau\cdot\ln\left(\frac{2^{(n+1)}V_g(N)}{V_R}\right)$$

Steady state current command

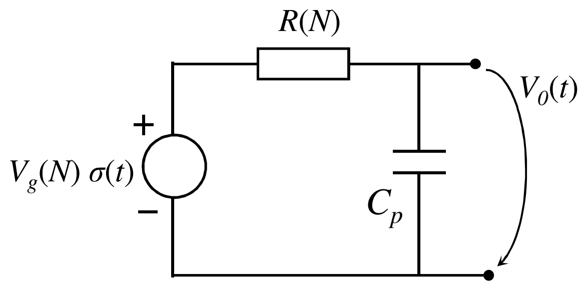
$$V_0(N)=-\frac{R}{R(N)}\cdot V_g(N)=-V_g(N)$$



voltage command



current command



Binary-Weighted Resistor DAC (cont'd)

Disadvantages:

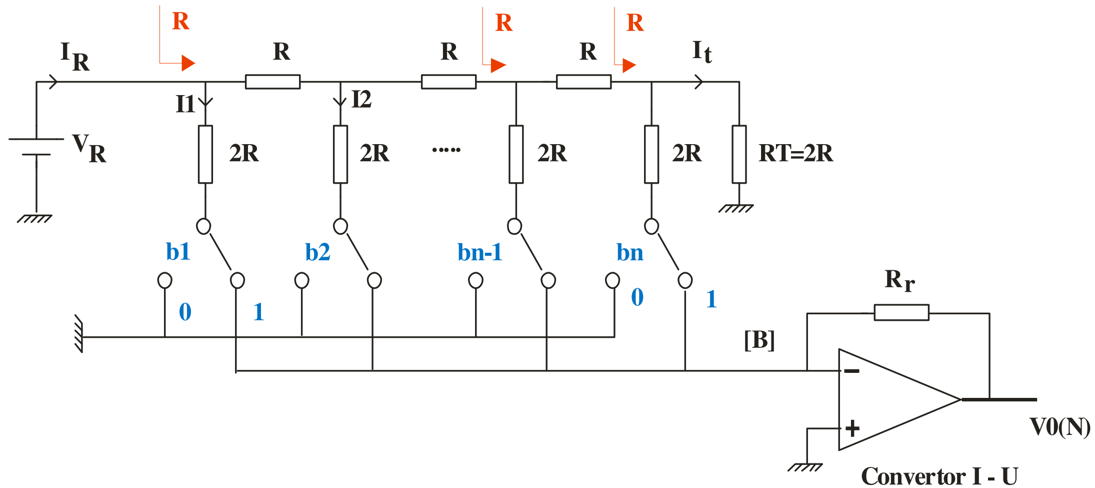
- Resistance Values Require Great Accuracy:
  e.g. Tolerance of R must be < $1/2^n$

- Often limited to 4-Bit conversions because of the limited current range possible with resistors;

- Larger bit numbers difficult due desired current changes being close in magnitude to noise amplitudes (for less significant bits);

- Hardware difficult realization for large bits number (due the weight inaccuracy for the large range);

R-2R ladder network DAC



$$I_k = \frac{2R}{2R+2R} \cdot I_{k-1} = 2^{-k}\frac{V_R}{R} = 2^{-k} I_R$$

$$V_0(N) = -R_r I(N)$$

$$I(N) = \sum_{k=1}^{n} I_k = \frac{1}{R} V_R \sum_{k=1}^{n} b_k 2^{-k} \quad \Rightarrow \quad V_0(N) = -\frac{R_r}{R} V_R \sum_{k=1}^{n} b_k 2^{-k}$$

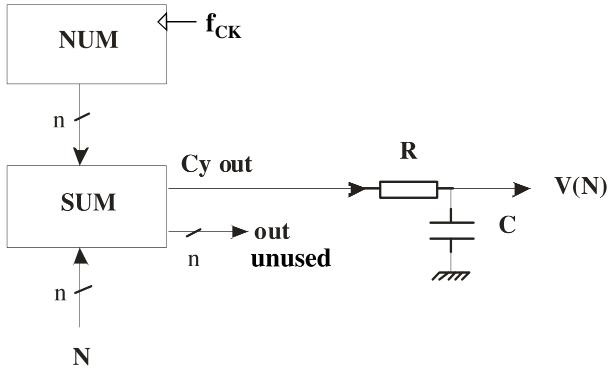
$$V_{0\_max}(N=0\ldots0\text{h}) = 0\text{V} \qquad V_{0\_min}(N=F\ldots F\text{h}) = -\frac{R_r}{R} \cdot V_R \cdot \left(1-2^{-n}\right)$$

$$\delta V = V_0(N=0\ldots1\text{h}) = -\frac{R_r}{R} \cdot V_R \cdot 2^{-n}$$

R-2R ladder network resistor DAC (cont'd)

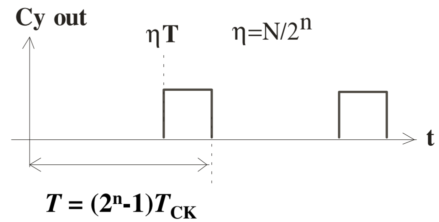
- Maintains constant current through all branches = no voltage transients;
- Less hardware constrain (easy to find R-2R resistor pair values);
- Faster response time due to lack of voltage transients.

Stochastic DAC (without resistor network)



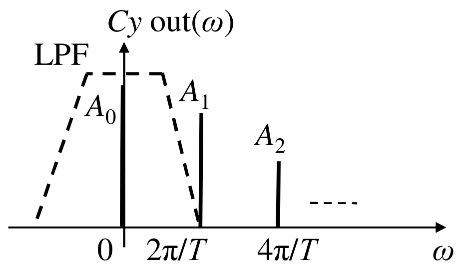
$$C_{y\,out}(t)=A_0+\sum_{k=1}^{\infty}A_k\cos\left(k\frac{2\pi}{T}t+\phi_k\right)$$

$$T=\left(2^n-1\right)T_{CK}$$



$$\left|H(f)\right|=\left|\frac{1}{1+j2\pi fRC}\right|=\frac{1}{\sqrt{1+\left(\frac{f}{f_T}\right)^2}}\qquad f_T=\frac{1}{2\pi RC}\ll\frac{1}{T}$$

$$V(N)=A_0=\frac{\tau}{T}E=\frac{N_1}{2^n-1}E=\frac{2^n E}{2^n-1}N=V_R\sum_{k=1}^{n}b_k 2^{-k}$$



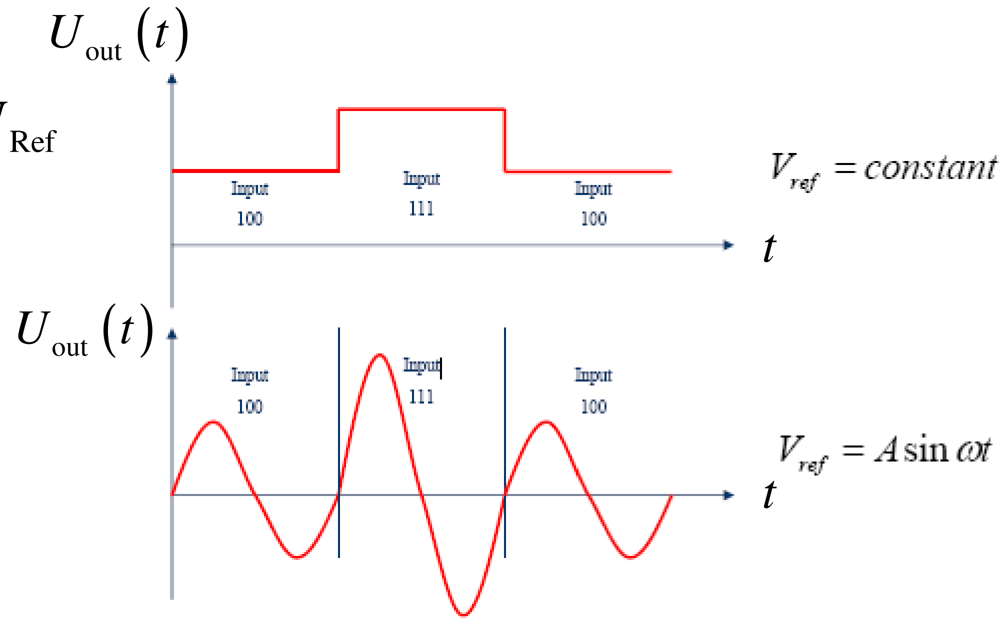
N sub-unitary number (N_1 supra-unitary)

Multiplying DAC

- slow time varying **external** U_{Ref}

$$U_{\mathrm{Ref}} = U_{in}(t)$$

$$\left.\frac{\mathrm{d}U_{in}(t)}{\mathrm{d}t}\right|_{\max} << \frac{\delta U_{\mathrm{o}}}{2 \cdot t_{\mathrm{conv}}}$$



- binary code on digital input → command for controlled amplification / attenuation;
- $U_{in}(t)$ must preserve DAC functionality;

DAC applications

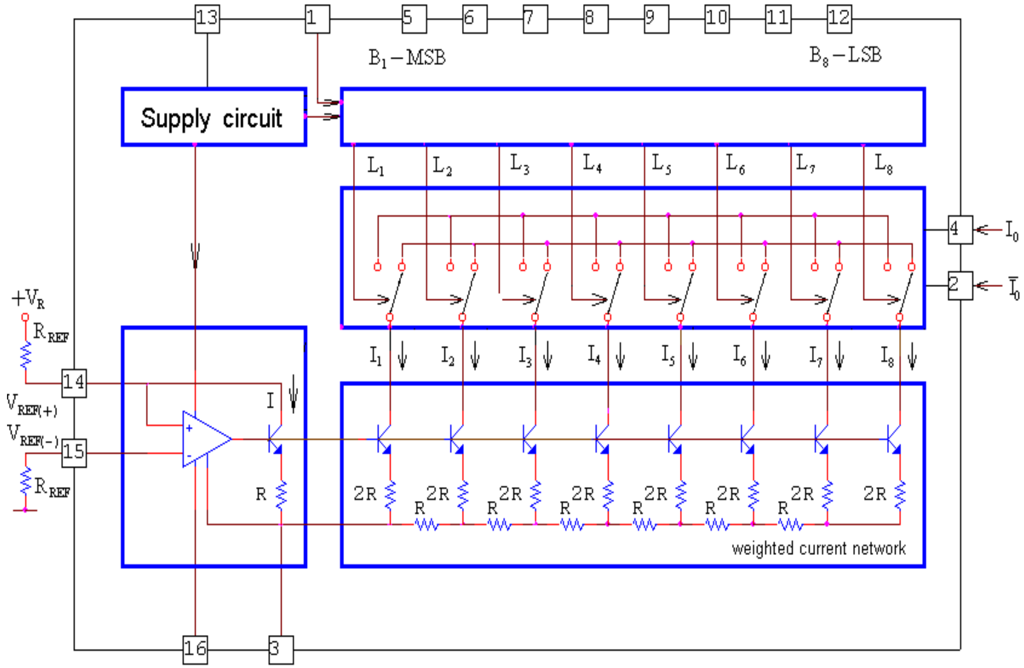
- Industrial Control Systems
  e.g. motor speed & valves;
- Digital Audio
  e.g. CD player;
- Digital Communications
  e.g. digital telephone and video systems;
- Waveform Function Generators
  e.g. direct digital synthesizer (DDS);

Example 1: Digital to analog converter (8 bits) - DAC 08

$I_k = 2^{-k} \cdot I$

$$I'_0(N)=\sum_{k=1}^{n} I'_k = \frac{V_R}{R_{ref}} \sum_{k=1}^{n} (1-b_k) 2^{-k}$$

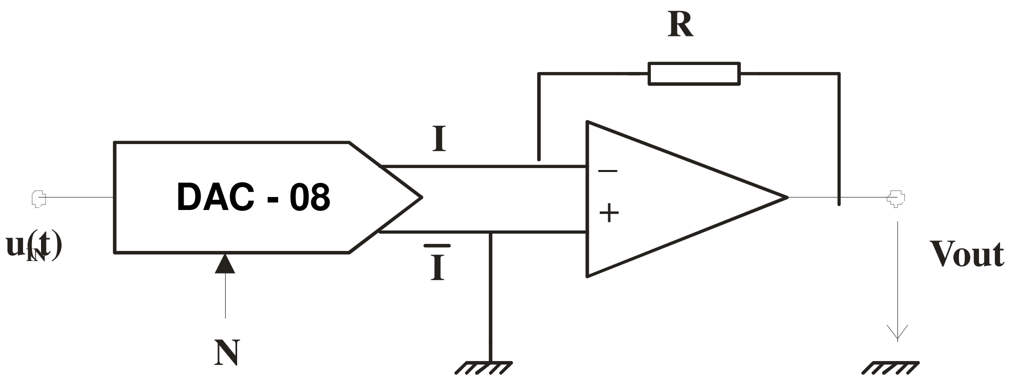
$$I_0(N)=\sum_{k=1}^{n} I_k = \frac{V_R}{R_{ref}} \sum_{k=1}^{n} b_k 2^{-k}$$



$$I'_{0\_min}(N=FFh)=0 \qquad I'_{0\_max}(N=00h)=\frac{V_R}{R_{ref}}\left(1-2^{-8}\right) \qquad \delta I'_0 = -\frac{V_R}{R_{ref}} \cdot 2^{-8}$$

$$I_{0\_min}(N=00h)=0 \qquad I_{0\_max}(N=FFh)=\frac{V_R}{R_{ref}}\left(1-2^{-8}\right) \qquad \delta I_0 = +\frac{V_R}{R_{ref}} \cdot 2^{-8}$$

Example 2: Inversion amplifier with digital adjustment gain



$$v_{out} = -RI(N)$$

$$v_{out}(t) = -u_{in}(t) \cdot \frac{R}{R_{ref}} \cdot \sum_{k=1}^{n} b_k 2^{-k} = A_u(N) \cdot u_{in}(t)$$

$$A_u(N) = -\frac{R}{R_{ref}} \cdot \sum_{k=1}^{n} b_k 2^{-k}$$

Analog to Digital Converter

- Function: converts input analog signal into a digital signal;
- ADC conversion comprises :
  - **Time sampling**: samples are taken from the analog signal (sampling frequency) and its values are maintained for a certain time interval;
  - **Quantization** : rounding off of the sampled value to the nearest of a limited number of digital values;
  - **Binary coding**: conversion of the quantized value into a binary code;

Sampling and quantization operation may lead to loss of information.

Under certain conditions ADC loss can be limited to an acceptable minimum;

Analog to Digital Converter

- Mathematical representation of ADC function:

$$f_{ADC}:\mathbf{R}\rightarrow N$$

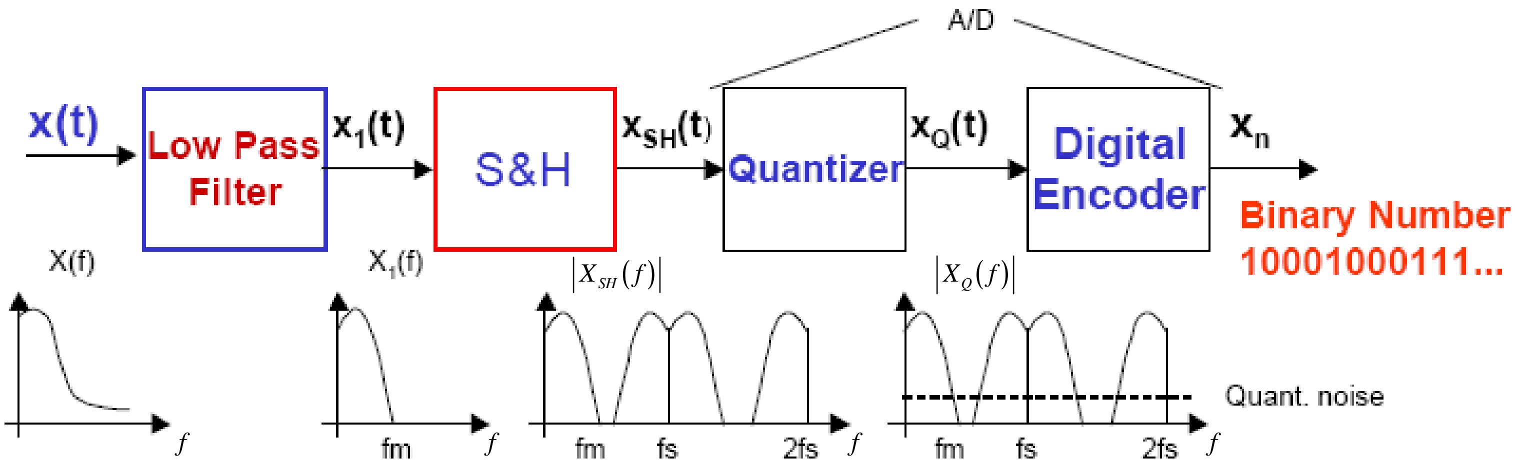
- Parameters:
  - Conversion type: unipolar, bipolar;
  - Quantization type: truncate, round, round-ceiling;
  - Binary code (natural, offset, two's complement, etc.);
  - Input type (U, I);
  - Input range;
  - Resolution - the smallest change required in the ADC analog input to surely change its output code by one level;
    - number of bits used for binary cod *(n);*
  - Conversion time - required time before the converter can provide valid output data
  - Accuracy of conversion - the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code

- Parameters (cont'd)
  - Converter Throughput Rate - the number of times the input signal can be sampled maintaining full accuracy

    - Inverse of the total time required for one successful conversion

    - Inverse of conversion time if no S/H (Sample and Hold) circuit is used;
- ADC Interface Signals :
  - Data: Digital I/O pins the ADC uses to supply data
    - Parallel output – n+1 pins (fast transmission, short distances)
    - Serial output – 2 pins (for long distances, need a internal shift-register)
  - Start: Pulse high to start conversion (input)
  - EOC (End of Conversion): Typically active low → low level of pulse indicate complete conversion (output value can be read);
  - Clock: Clock used for conversion (for synchronising ADC sub-blocks, for internal FSM);

A/D Converter – traditional data converter at Nyquist rate ($f_s > 2f_m$)

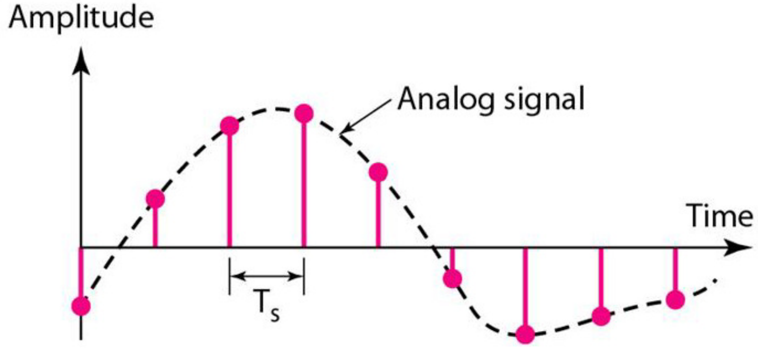


Successive operations for AD conversion process.

ADC introduces a non-compensable quantization noise.

Sampling process (remember)

- continuous signal conversion into a discrete time samplers sequence (ideal sampling, natural sampling, flat-top sampling);



▪ Ideal sampling

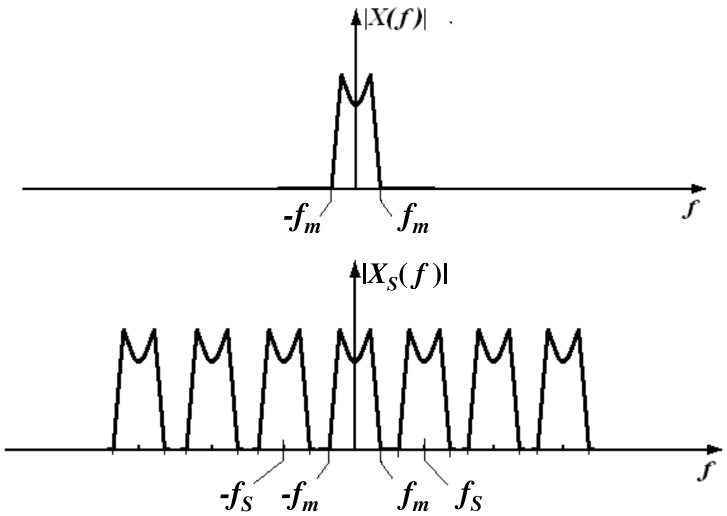
$$x(t) \rightarrow x_s(t) = x[n] = x(nT_s) \in R$$

$$x_s(t) = \sum_{n=-\infty}^{+\infty} x(t) \cdot \delta(t - nT_S) = x(t) \cdot \delta_{T_S}(t)$$

$$\delta_{T_S}(t) = \frac{1}{T_S} \sum_{n=-\infty}^{+\infty} e^{jn\frac{2\pi}{T_S}t}$$

$$X_S(f) = \mathcal{F}\{x(t) \cdot \delta_{T_S}(t)\} = X(f) \otimes \frac{1}{T_S} \sum_{n=-\infty}^{+\infty} \delta\left(f - \frac{n}{T_S}\right)$$

$$= \frac{1}{T_S} \sum_{n=-\infty}^{+\infty} X\left(f - \frac{n}{T_S}\right) = f_S \cdot \sum_{n=-\infty}^{+\infty} X(f - n \cdot f_S)$$



Sampling process (cont'd)

▪Natural sampling

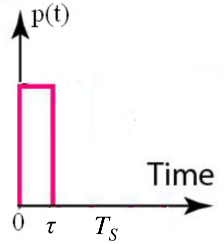
$$x(t) \rightarrow x_s(t) = x(t)\,p_{T_S}(t)$$

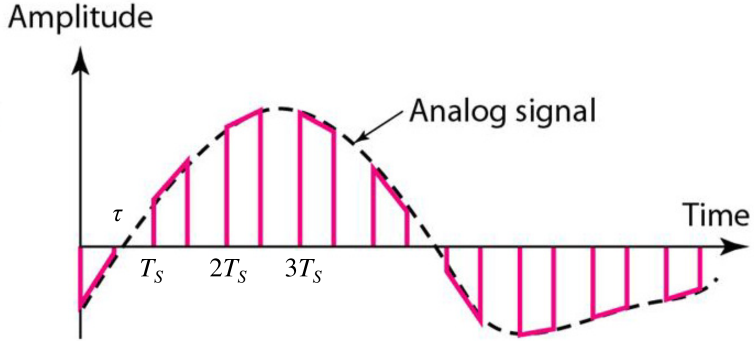
$$p_{T_S}(t) = \sum_{n=-\infty}^{+\infty} P_n \cdot e^{jn\frac{2\pi}{T_S}t}$$

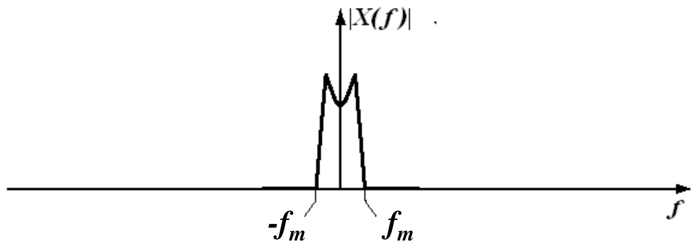
$$P_n = \frac{1}{T_s}\int_0^{T_S} p_{T_S}(t)\cdot e^{-j\frac{2\pi n}{T_S}t}\,\mathrm{d}t$$

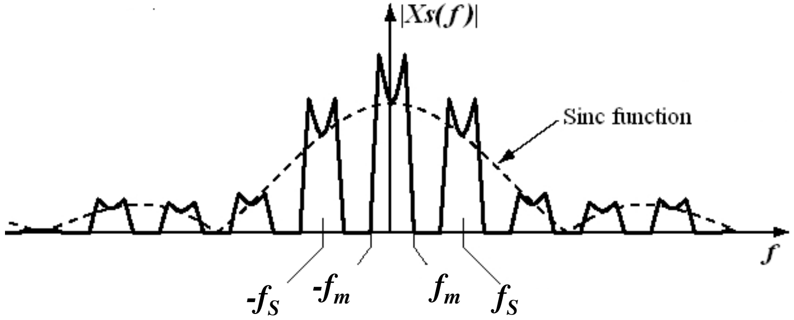
$$= \frac{\tau}{T_S}\cdot e^{-j\frac{2\pi\cdot n\cdot\tau}{2T_S}}\cdot \mathrm{sinc}\left(\frac{n\cdot\pi\cdot\tau}{T_S}\right)$$

$$X_S(f) = \mathcal{F}\{x(t)\cdot p_{T_S}(t)\} = \sum_{n=-\infty}^{+\infty} P_n \cdot X\left(f - \frac{n}{T_S}\right)$$



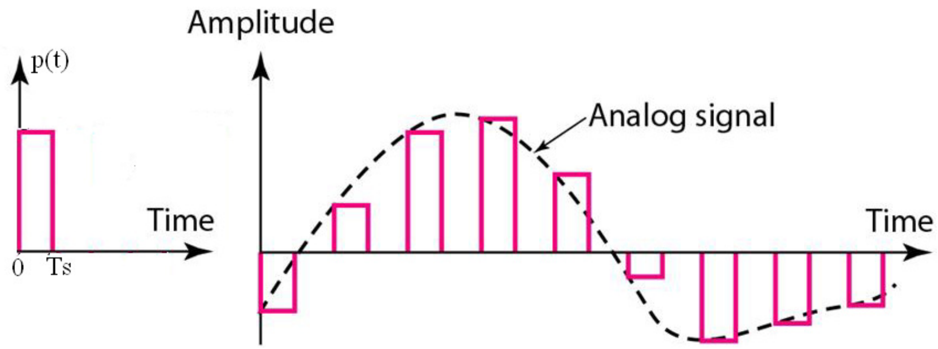






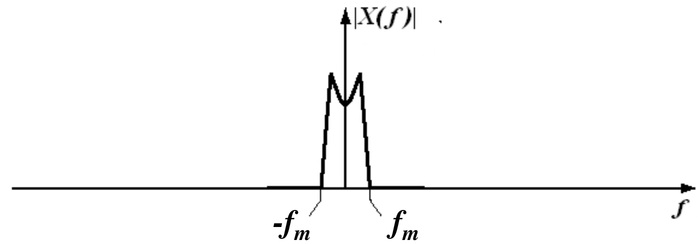
Sampling process (cont'd)

▪Flat-top sampling

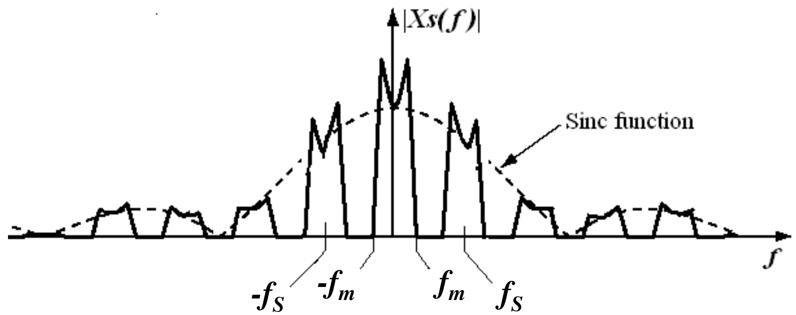


$$x(t) \rightarrow x_s(t) = \left\{ x(t) \sum_{n=-\infty}^{+\infty} \delta(t - nT_S) \right\} \otimes p(t)$$

$$P(f) = \mathcal{F}\{p(t)\} = T_S \cdot e^{-j\pi f T_S} \cdot \mathrm{sinc}(\pi f T_S)$$



$$X_S(f) = \cdot e^{-j\pi f T_S} \cdot \mathrm{sinc}(\pi f T_S) \cdot \sum_{n=-\infty}^{+\infty} X\left(f - \frac{n}{T_S} \right)$$



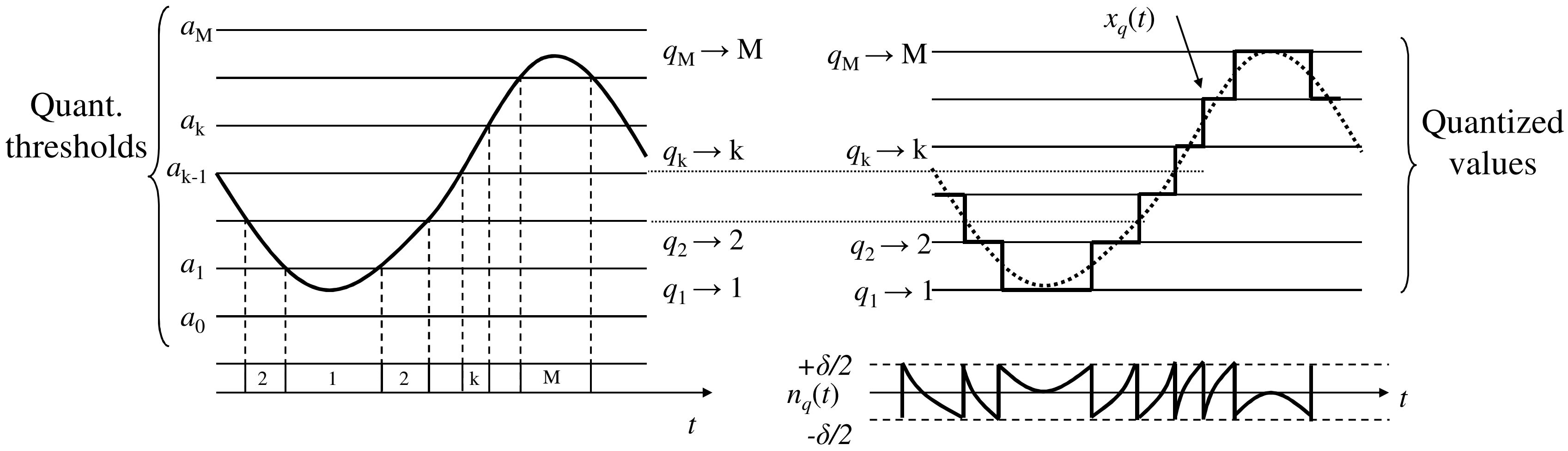
Sampling rate is given in Samples/s

(S/s, kS/s, MS/s, GS/s);

Quantizing process

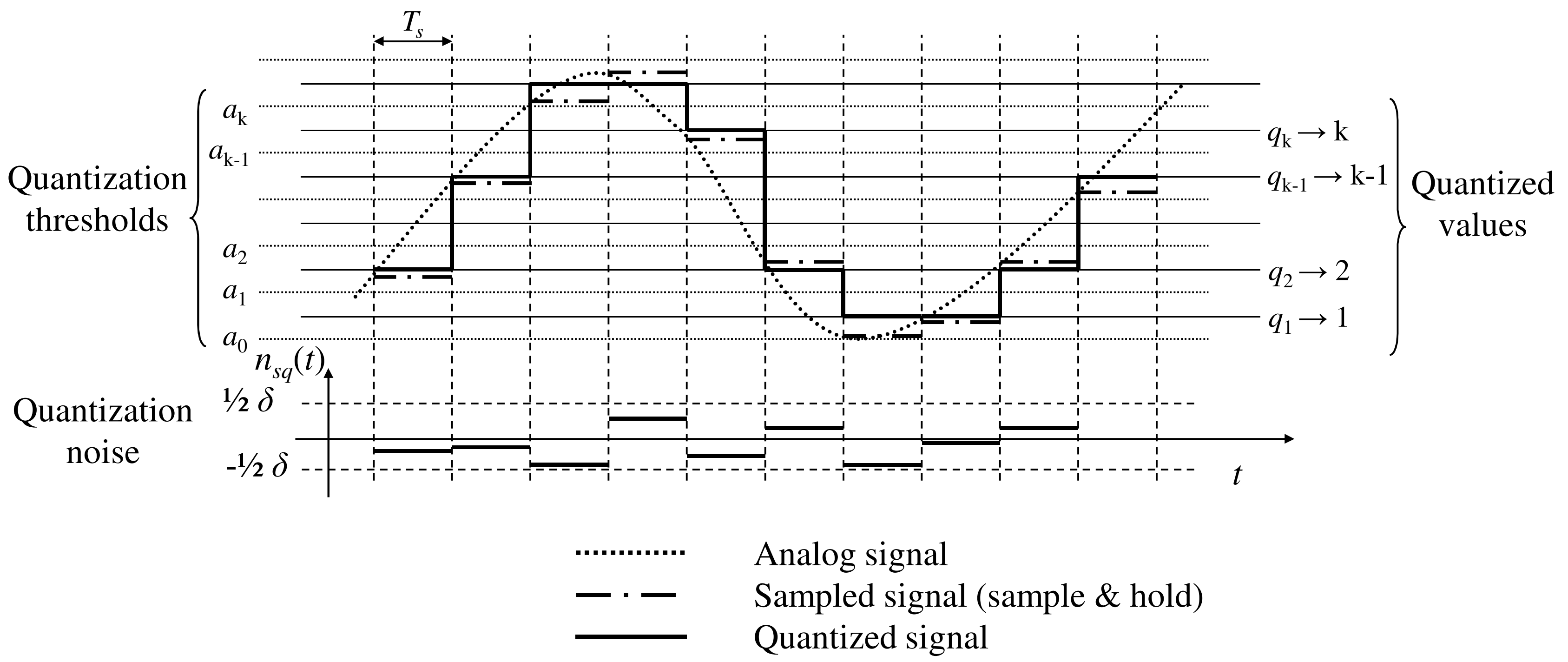
- analog signal approximation to the nearest discrete value:

$$x[n] \rightarrow x_q[n] = q_k \Rightarrow k, \quad k \in \overline{1, M}, \quad q_k \in Q_M$$



Quantization of non-sampled signal (continuous)

Sampling & quantizing process



- Quantization – uniform (constant step) – linear ADC

  – non-uniform (variable step) – nonlinear ADC

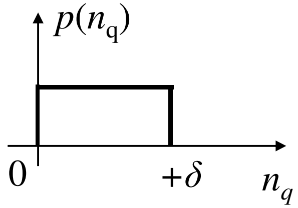
Quantization

Truncating quantization $q_k = a_{k-1}$

$$U_{qt} = U_{ref} \sum_{i=1}^{n} 2^{-i} b_i = \delta U \sum_{i=1}^{n} 2^{n-i} b_i = N_t \delta U$$

Quantization noise

$$n_{qt} = U - U_{qt} = U_{ref} \sum_{i=n+1}^{\infty} 2^{-i} b_i$$

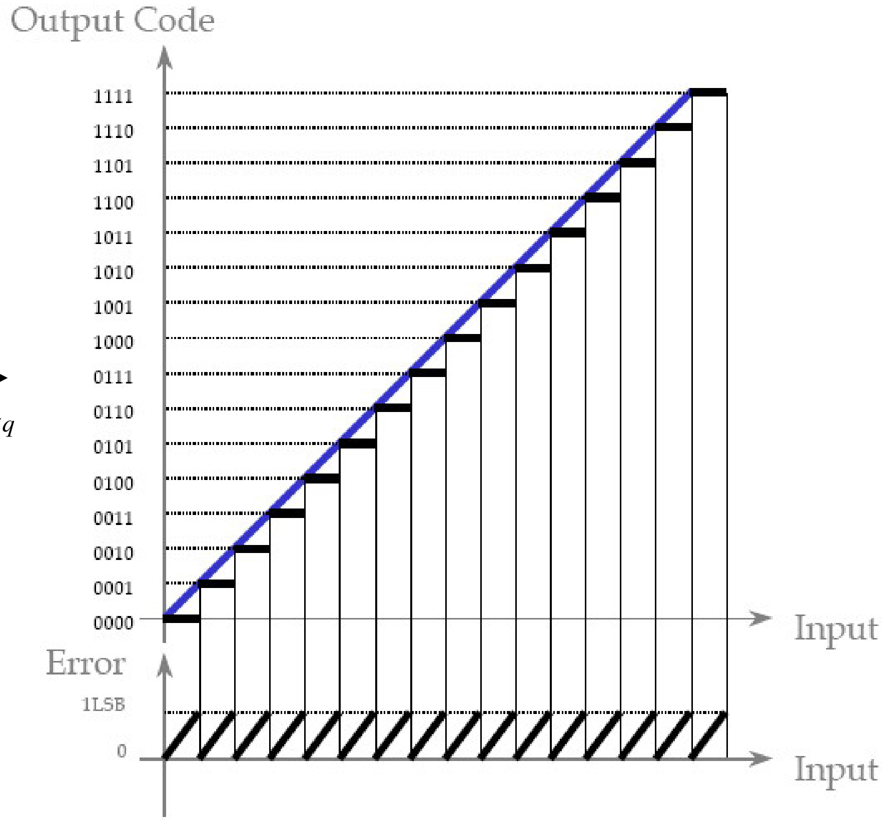


Noise mean value

$$E\{n_{qt}\} = \int_{-\infty}^{\infty} p(n_{qt}) n_{qt} dn_{qt} = \int_{0}^{\delta} n_{qt} \frac{1}{\delta} dn_{qt} = \frac{\delta}{2}$$

Noise variance (power)

$$\sigma_{qt}^2 = E\{n_{qt}{}^2\} - [E\{n_{qt}\}]^2 = \frac{\delta^2}{12} = \frac{2^{-2n}}{12} U_{ref}^2$$



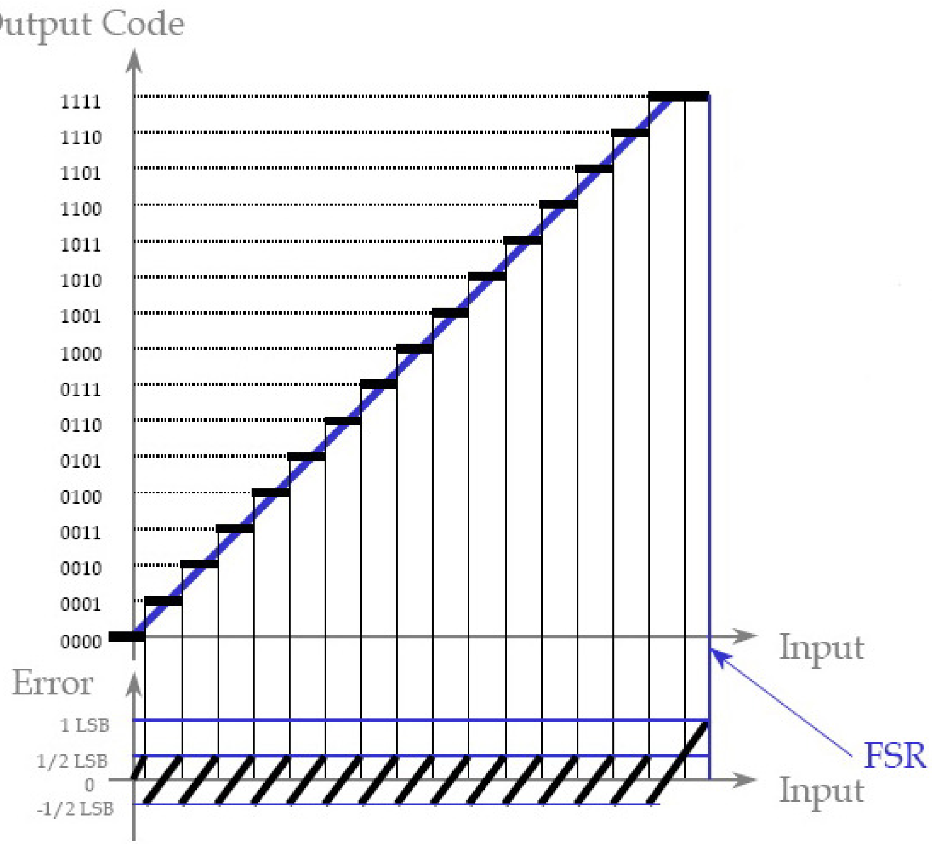
Ideal characteristic

Quantization (cont'd)

Rounding quantization $q_{k+1} = \dfrac{a_k + a_{k+1}}{2}$

$$U_{qr} = \delta U \cdot b_{n+1} + U_{qt} = U_{ref}\left(2^{-n} b_{n+1} + \sum_{i=1}^{n} 2^{-i} b_i\right)$$

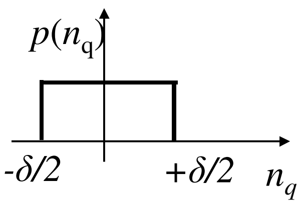
$$= (N_t + b_{n+1})\delta U = N_r \delta U \ , \ b_{n+1} \in \{0,1\}$$



Ideal characteristic

Quantization noise

$$n_{qt} = U - U_{qt} = U_{ref}(-2^{-(n+1)} b_{n+1} + \sum_{i=n+2}^{n} 2^{-i} b_i)$$



Noise mean value

$$E\{n_{qr}\} = \int_{-\delta/2}^{+\delta/2} n_{qr} \frac{1}{\delta} dn_{qr} = 0$$

Noise variance (power) $\sigma_{qr}^2 = E\{n_{qr}{}^2\} - [E\{n_{qr}\}]^2 = \dfrac{\delta^2}{12} = \dfrac{2^{-2n}}{12} U_{ref}^2$

Quantization (cont'd)

Round-ceiling quantization $q_k = a_k$

$$U_{qm} = \delta U + U_{qt} = U_{ref}(2^{-n} + \sum_{i=1}^{\infty} 2^{-i} b_i)$$

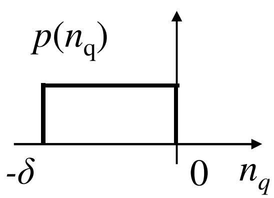
$$= (N_t + 1)\delta U = N_m \delta U$$

Quantization noise

$$n_{qm} = U - U_{qm} = U_{ref}(-2^{-n} + \sum_{i=n+1}^{\infty} 2^{-i} b_i)$$

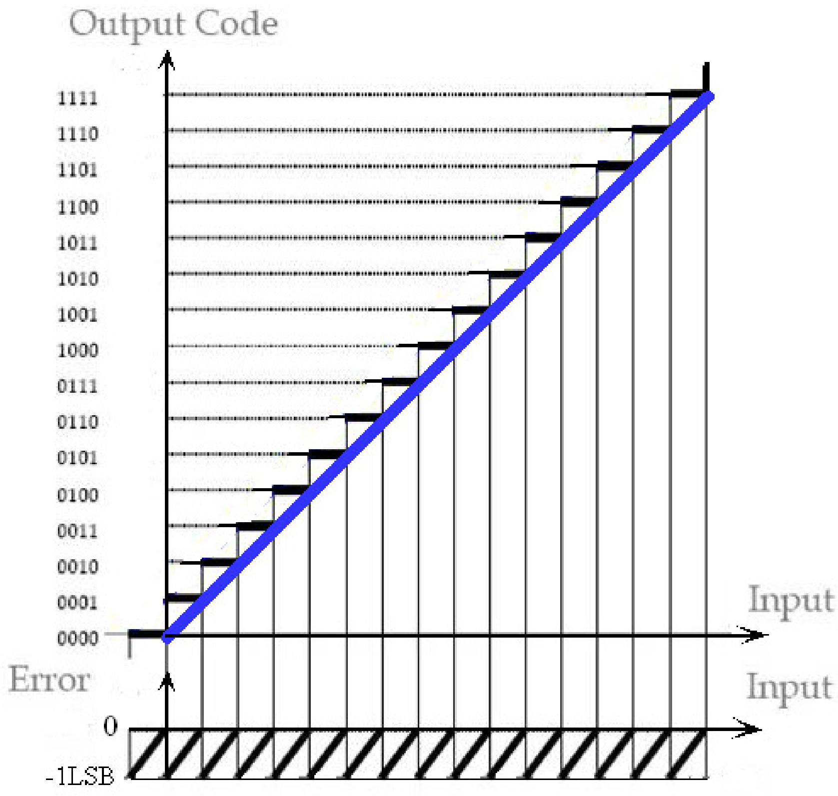
Noise mean value

$$E\{n_{qm}\} = \int_{-\delta}^{0} n_{qm} \frac{1}{\delta} \, \mathrm{d}\, n_{qm} = -\frac{\delta}{2}$$



Noise variance (power)

$$\sigma_{qm}^2 = E\{n_{qm}{}^2\} - [E\{n_{qm}\}]^2 = \frac{\delta^2}{12} = \frac{2^{-2n}}{12} U_{ref}^2$$



Ideal characteristic

Quantization (cont'd)

Noise value as: voltage (rms, p-p), LSB (rms, p-p), SNR;

Signal to quantization noise ratio (SNR_q)

Considering a periodic signal at input, with period *T*, having average power:

$$P_x = \frac{1}{T}\int_0^T x^2(t)\,\mathrm{d}t = U^2_{x\_ef}$$

$$SNR_q(n) = 10\cdot\log\left(\frac{P_x}{P_{n_q}}\right) = 10\cdot\log\left(\frac{U^2_{x\_ef}}{\sigma_q^2}\right) = 10\cdot\log\left(\frac{12\cdot U^2_{x\_ef}}{\delta^2}\right) = 10\cdot\log\left(2^{2n}\cdot\frac{12\cdot U^2_{x\_ef}}{U^2_{ref}}\right)$$

$$= 6{,}02\cdot n + 10{,}8 + 20\cdot\log\left(\frac{U_{x\_ef}}{U_{ref}}\right) \quad [\mathrm{dB}]$$

Total SNR after quantization process:

For analog noisy signal, the total noise power is $\sigma_T^2 = \sigma_a^2 + \sigma_q^2$

effective bit number : $n_{ef} = \log_4\frac{U^2_{x\_ef}}{\sigma_T^2} = n - \log_4\left(1 + \frac{\sigma_a^2}{\sigma_q^2}\right)$

Quantization (cont'd)

Example: a full range sine wave input $x(t) = U_0 \sin(\omega t)$ $U_0 \cong \frac{U_{ref}}{2}$

Signal power and rms value: $P_x = \frac{1}{T}\int_0^T x^2(t)\,\mathrm{d}t = \frac{U_0^{\,2}}{2} = U_{x\_ef}^2 = \frac{U_{ref}^2}{8}$

$$SNR_q(n) = 10\cdot\log\left(\frac{P_x}{P_{n_q}}\right) = 10\cdot\log\left(\frac{A^2}{2\sigma_q^2}\right) = 10\cdot\log\left(\frac{6A^2}{\delta^2}\right) = 10\cdot\log\left(\frac{3\cdot U_{ref}^2}{2\cdot 2^{-2n}U_{ref}^2}\right)$$

$$SNR_q(n) = 6.02\cdot n + 1.76\text{ dB} \qquad \text{(for sinwave full range quantization)}$$

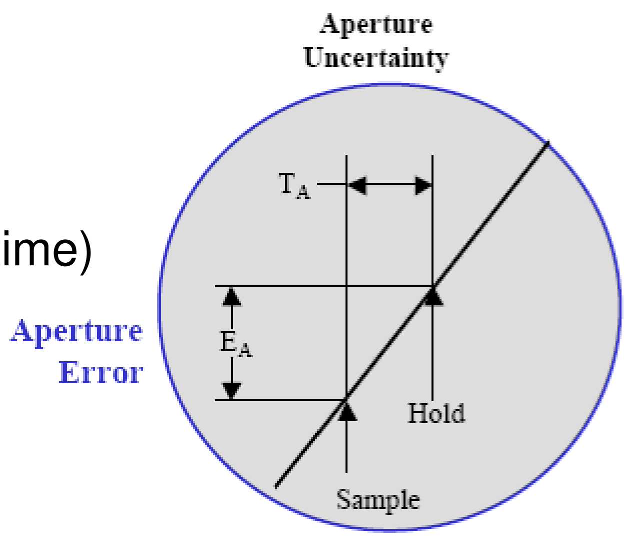
Dynamic range: $DR = 20\cdot\lg\frac{x_{\max}}{x_{\min}} = 20(n-1)\cdot\lg 2 \cong 6{,}02\cdot n - 6.02$

$ENOB = \left(SNR_q\big|_{\mathrm{dB}} - 1{,}76\right)/6.02$ bits number for specified SNR_q

Example: $SNR_q(10\text{ bit}) = 62\text{ dB}$

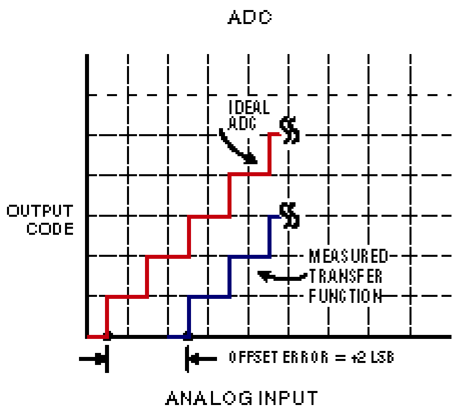
total effective bit number: $n_{ef} = \log_4\frac{U_0^2}{\sigma_T^2} + \log_4\frac{1}{3} = n - \log_4\left(1 + \frac{\sigma_a^2}{\sigma_q^2}\right)$

- **Non-ideality errors**
  - **Static errors**
    - Offset error (linear error);
    - Gain error (linear error);
    - Full-Scale error (offset error + gain error) ;
    - Integrated nonlinearity error (INL);
    - Differential nonlinearity error (DNL);
  - **Dynamic error**:
    - Aperture error (due to the delay between the clock signal of S/H block and the effective holding time)

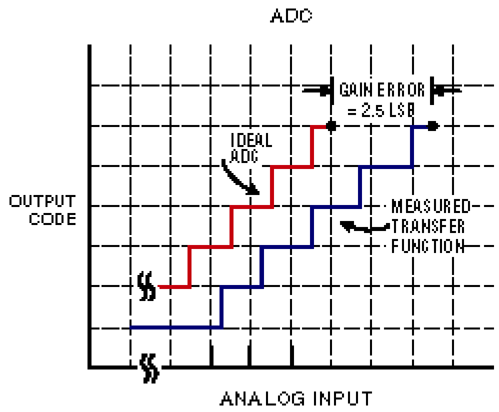


For sin wave input $x(t) = A\sin(\omega t)$

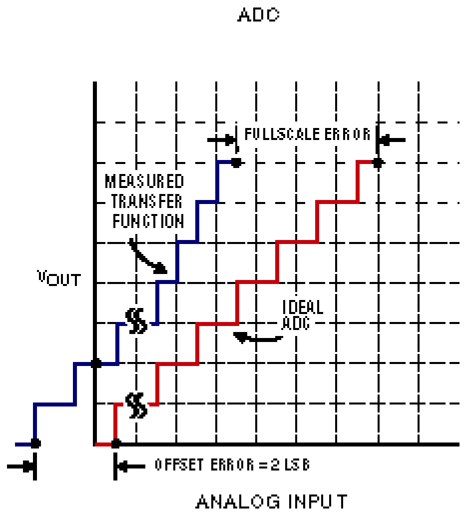
$$E_A = \left|\frac{dx(t)}{dt}\right| T_A < \frac{\delta V}{2} \Rightarrow T_A = \frac{1}{2^n \pi f}$$



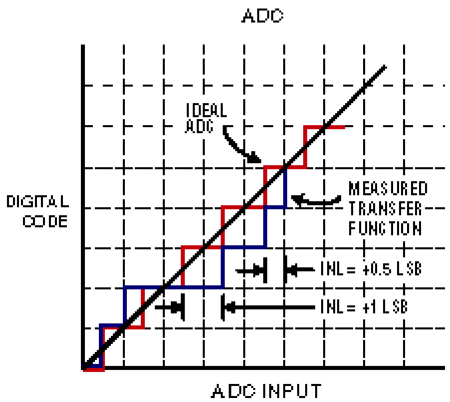
Offset error



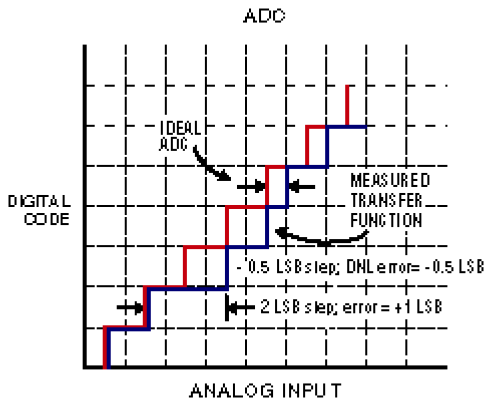
Gain error



Factor scale error



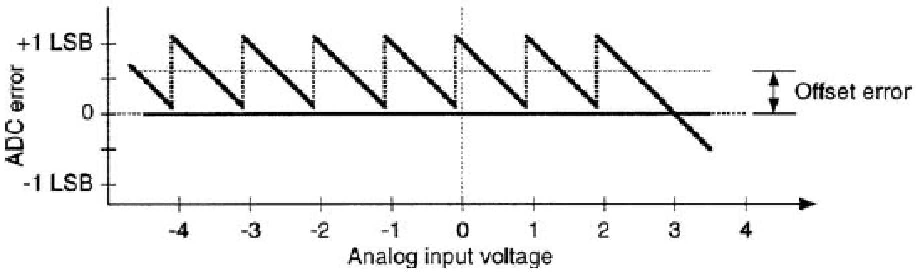
INL error



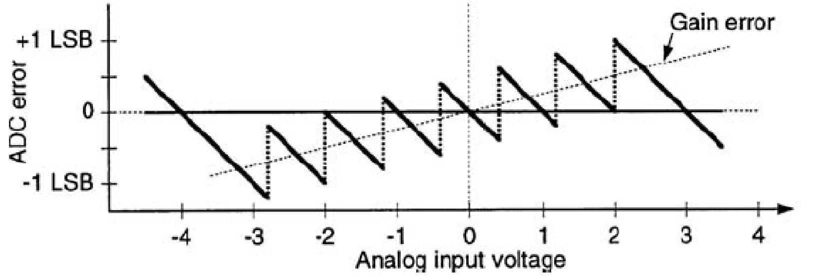
DNL error

❑ Effects of static errors and quantizing error (examples)

An ideal three-bit quantizer, with +0.6 LSB offset error



An ideal three-bit quantizer, with a gain of 1.25 instead of 1.00



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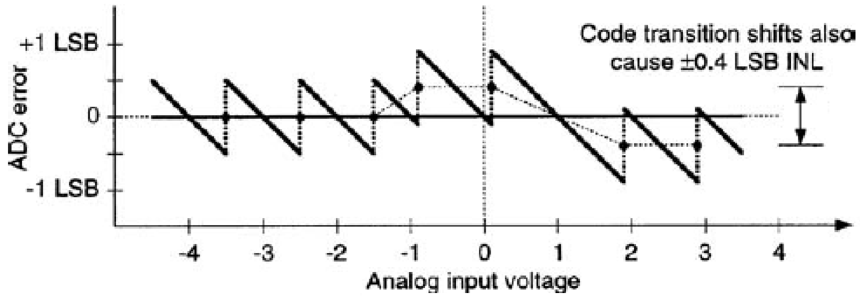
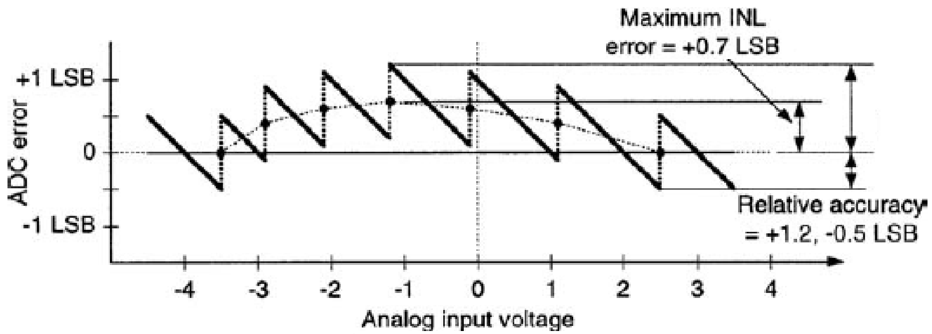
An ideal three-bit quantizer, with INL error caused by important DNL error

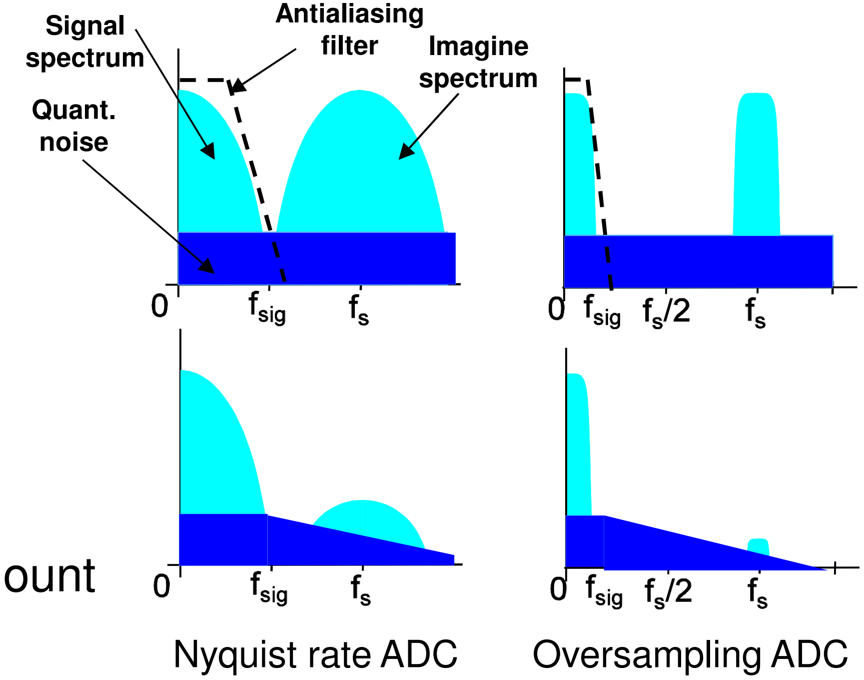


An ideal three-bit quantizer, with INL error and small DNL error



Improving A/D conversion techniques

Oversampling



OSR – oversampling ratio

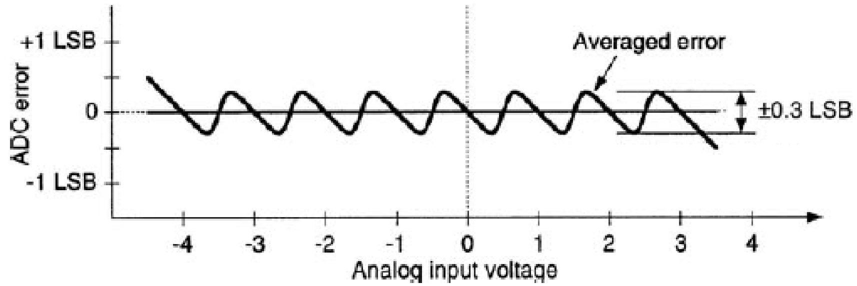
$$OSR = \frac{f_S}{f_{S\min}} = \frac{f_S}{2 \cdot f_{sig}}$$

$$SNR_q(n) = 6.02 \cdot n + 1.76 + 10 \cdot \log(OSR)$$

Dithering – adding a small amount

of random noise (maximum = 1/2·δU) to the input before conversion (for constant and slow varying analog signal).

LSB oscillates randomly between 0 and 1 in the presence of very low input levels.

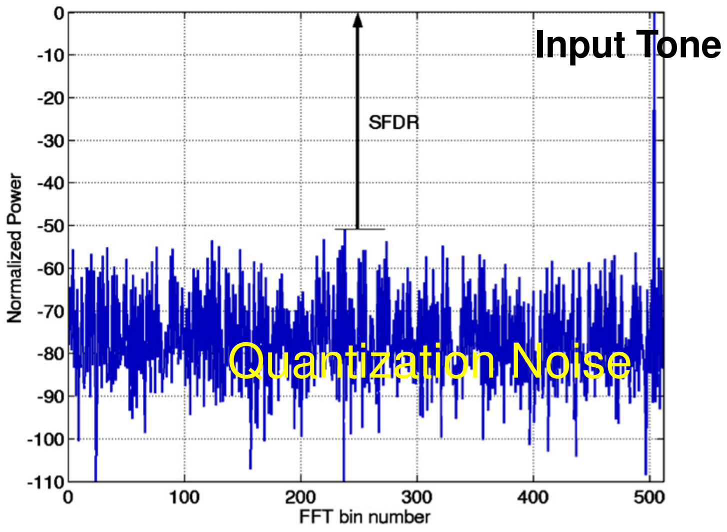


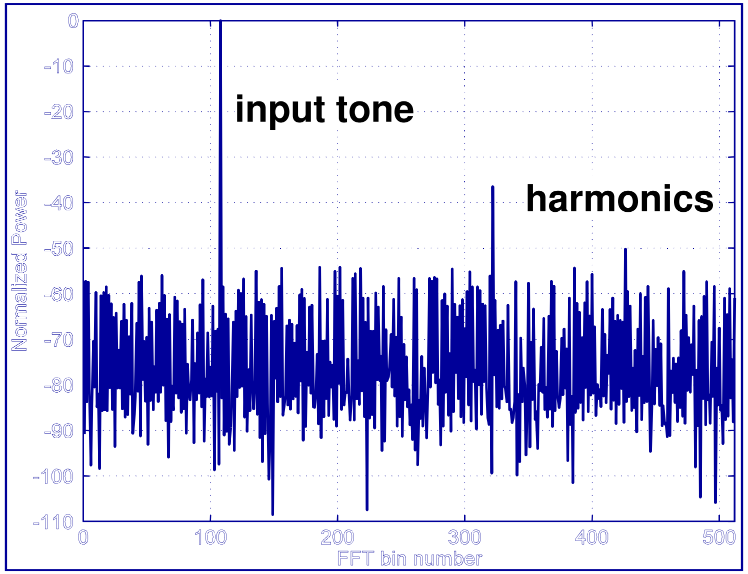
Acronyms for A/D converter

- SNR - Signal to (quantization) Noise Ratio = Signal power to noise power ratio (usually specified in dB);
- THD – Total Harmonic Distortion (due nonzero INL) = the ratio of the rms value of the fundamental sinewave signal to the mean value of the root-sum-square of its harmonics (usually the first five harmonics); Specified in dBc (decibels below *carrier*);
- SINAD (dBc) - Signal-to-Noise Plus Distortion ratio (same as SNDR) = ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics plus all noise components;
- SFDR - Spurious Free Dynamic Range = the ratio of the rms value of the signal to the rms value of the worst spurious spectral component (that may be or may not be an harmonic of the original signal);

Specified in dBc or in dBFS;

- ENOB - Effective Number of Bits: $n = \left[\left(SNR\,[\text{dB}] - 10{,}8\ \text{dB} - 20 \cdot \log\left(\frac{U_{x\_ef}}{U_{ref}} \right) \right) \Big/ 6{,}02 \right]$
- FOM – ADC Figure of Merit : $FOM = \frac{\text{Power}}{2^{\text{ENOB}} f_S}$ [Joule/level resolved]

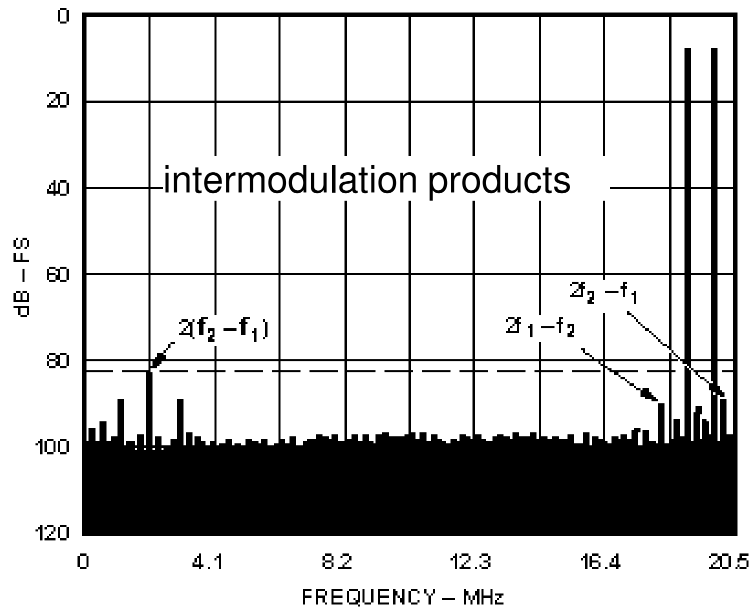




Other quantization impairments:

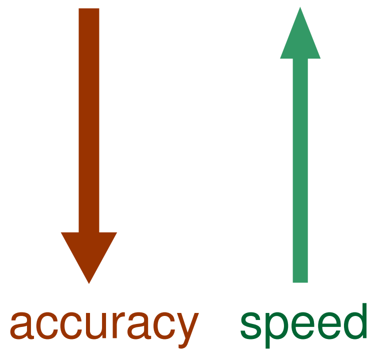
- SFDR
- Harmonics $m \cdot f_{sin} + n \cdot f_{sample}$

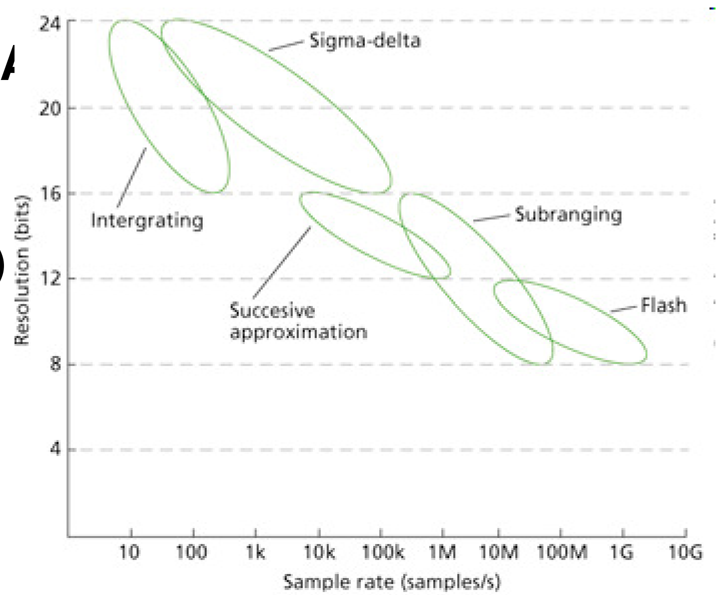
intermodulation products



A/D converter structures

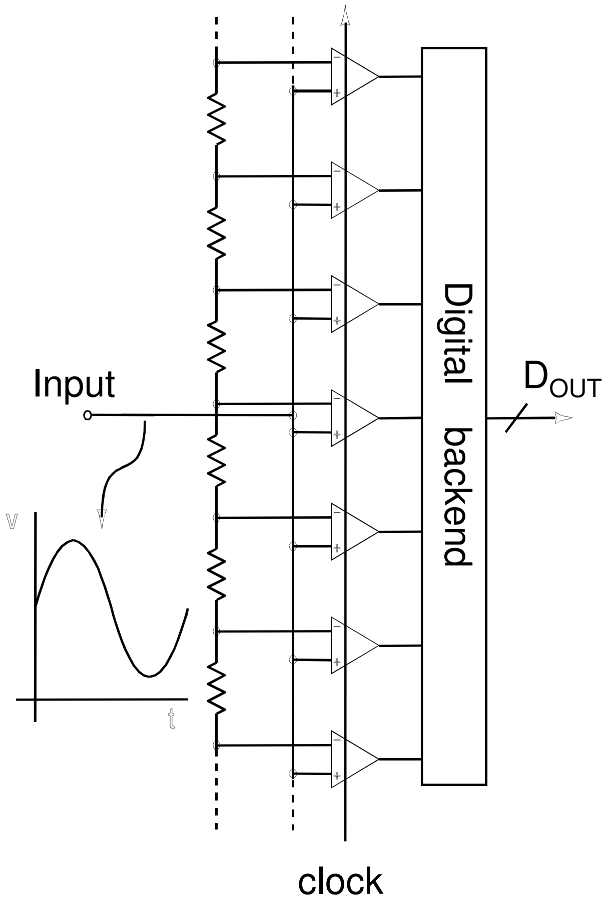
- Without integration
  - Without feedback
    - Flash ADC (direct conversion)
    - Folding ADC (Two-step ADC)
    - Pipelined ADC (serial ADC)
    - Time-interleaved ADC
    - Charged – coupled device ADC (CCD-A
    - Time-stretch ADC (optical ADC)
  - With feedback
    - Successive approximation ADC (SAR)
    - Ramp-compare ADC
    - Delta-encoded ADC
- With integration
    - Sigma-delta ADC
    - ADC with intermediate FM stage
    - Integrating ADC (single-slope, dual-slope, multiple slope)





Flash ADC

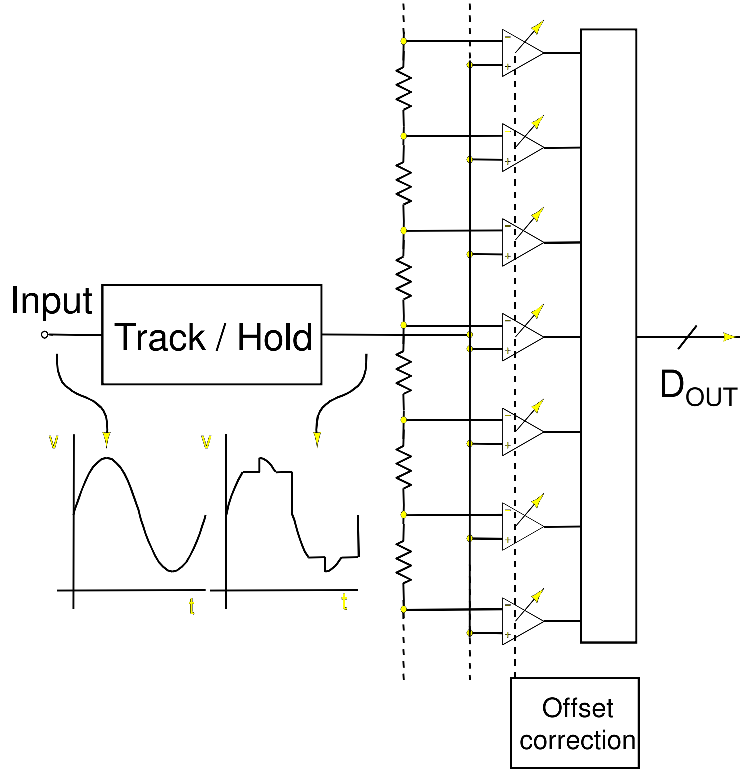
- bank of 2^n-1 parallel comparators (high complexity);
- very fast - GHz sampling rates (limited only by delays of comparators and logic network);
- references – resistor ladder
- few bits of resolution (4 – 8 bits, rarely 10 bits)
- high input capacitance
- expensive power / area (in IC)
- are prone to produce glitches (clock skew – comparators sample the inputs at different instants)
- high cost
- applications: video, wideband communications, optical storage



Flash ADC

Improving technique – track / hold

- T/H for good dynamic performance
- Offset correction in comparators



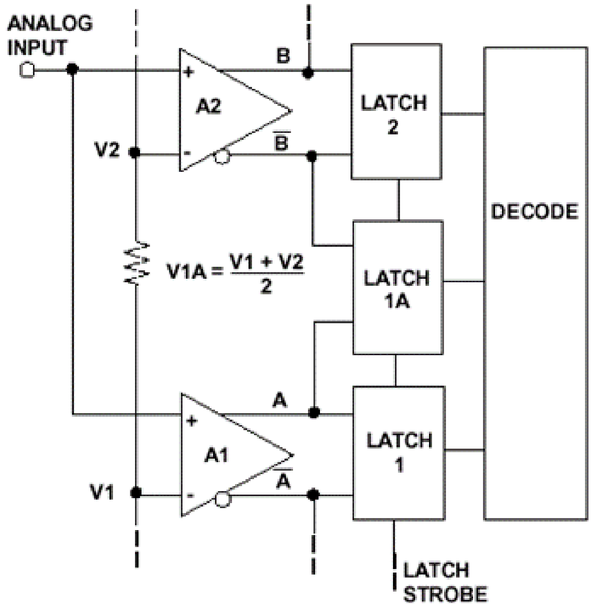
Example: AD9066 Dual 6-bit, 60MSPS Flash ADC

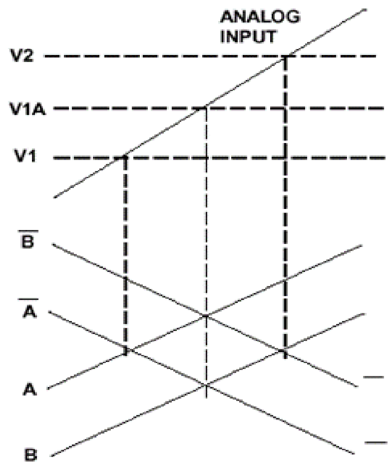
Key specifications:

- Input Range: 500mV p-p
- Input Impedance: 50kΩ || 10pF
- ENOB: 5.7 bits @15.5MHz Input
- On-Chip Reference
- Power Supply: Single +5V
- Package: 28-pin SOIC
- Ideal for Quadrature Demodulation

“Interpolating” Flash ADC

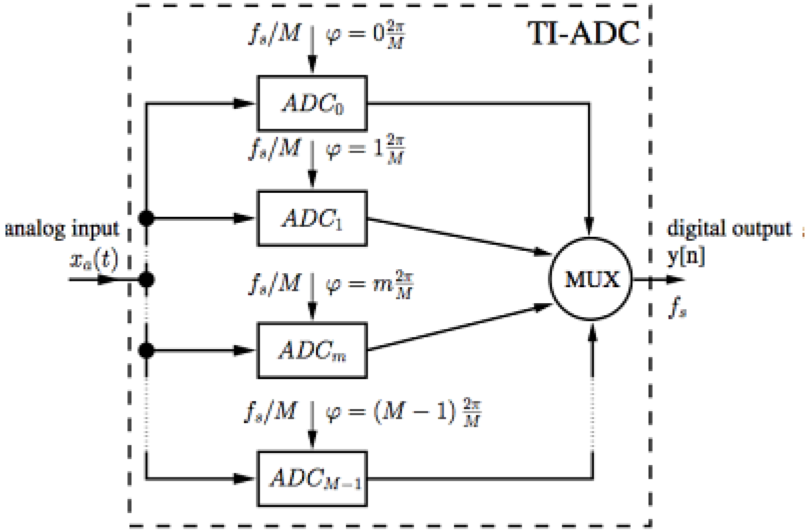
- reduces the number of comparator preamplifiers at the input of a Flash converter by a factor of two;
- substantially reduces the input capacitance, power dissipation, area of flash converters;
- preserves the one-step nature of a Flash architecture (VLSI technology);

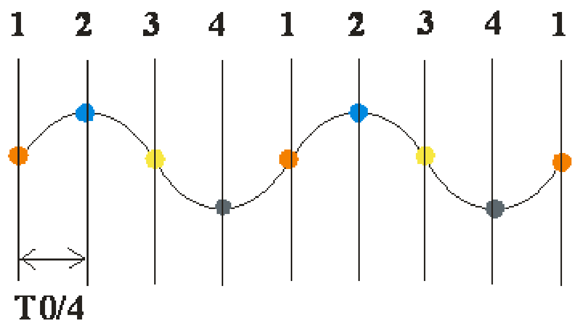




Time-interleaved ADC (TI-ADC)

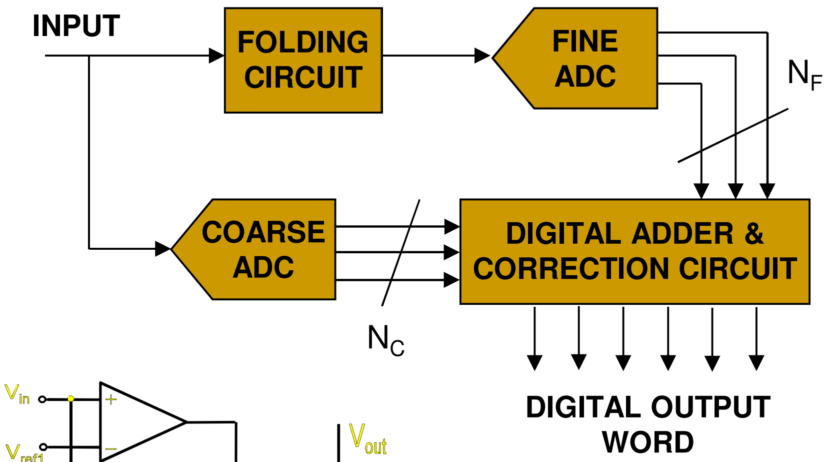
- uses M parallel flash ADCs;
- ADC sample data every M-th cycle of the effective sample clock;
- sample rate is increased M times;
- complexity is increased M times;
- requires correction of time-interleaving mismatch errors;
- applications: video, wideband communications, optical storage;

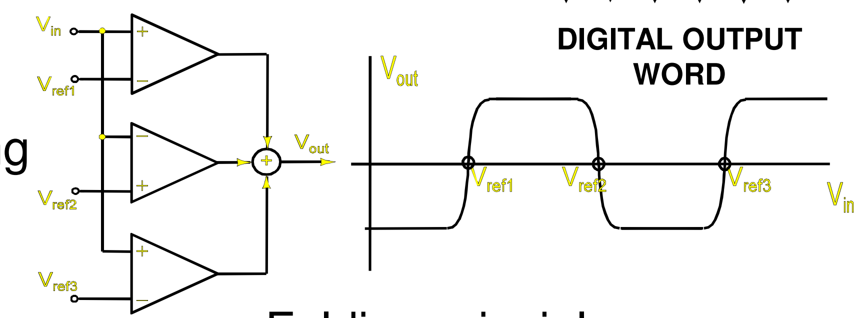




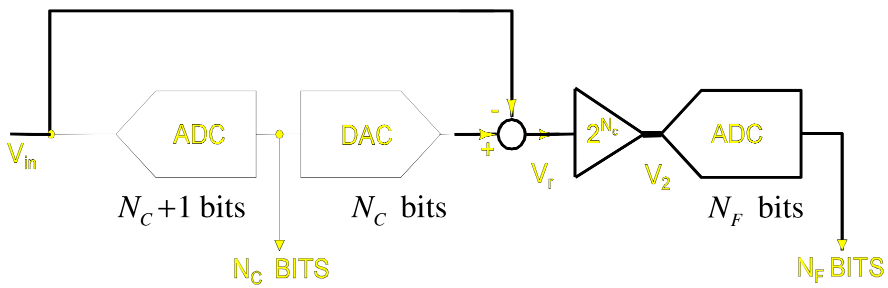
Folded Flash ADC (two steps)

- *Folding* = technique that reduces hardware
- maintaining the fast nature of a full Flash ADC;
- An analogue pre-processing circuit generates a residue which is digitised to obtain the LSBs;
- The MSBs are resolved using a coarse ADC that operates in parallel with the folding circuit;
- increase latency;
- Folded ADC reduces latches and logic: N_C+N_F bits need $2^{N_c}+2^{N_f}-2$ comparators;
- First stage determine the output sign;
- At every stage (except the last) the LSB is wasted;





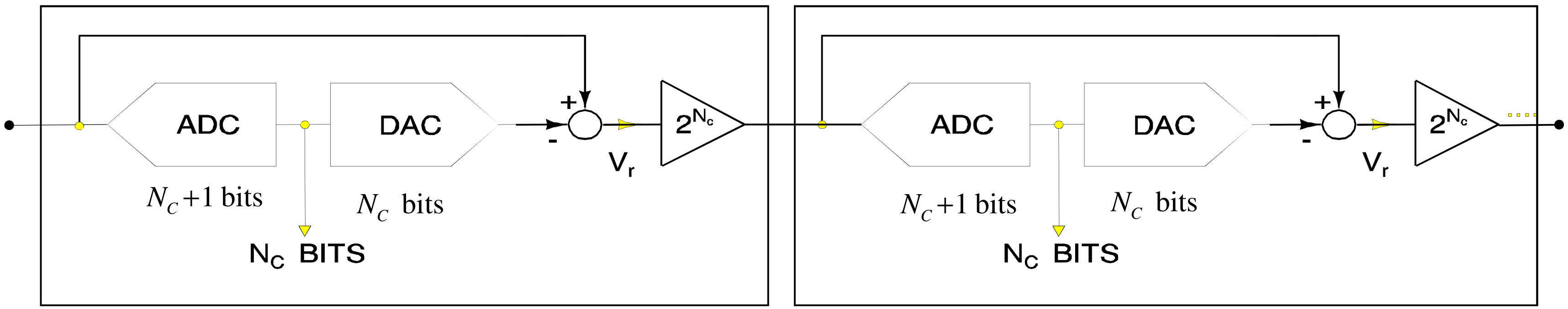
Folding principle



Serial/Parallel ADC (pipelined)

uses more steps of sub-ranging (with same bits number N_C);

- one stage
  - a coarse conversion is done
  - amplifies the difference of the input signal (determined with a DAC), then go to next stage
- fast conversion - GHz sampling rates;
- data latency greater than flash, but less than SAR
- high resolution with less complexity;
- ADC overload in next stage need Digital Error Correction;

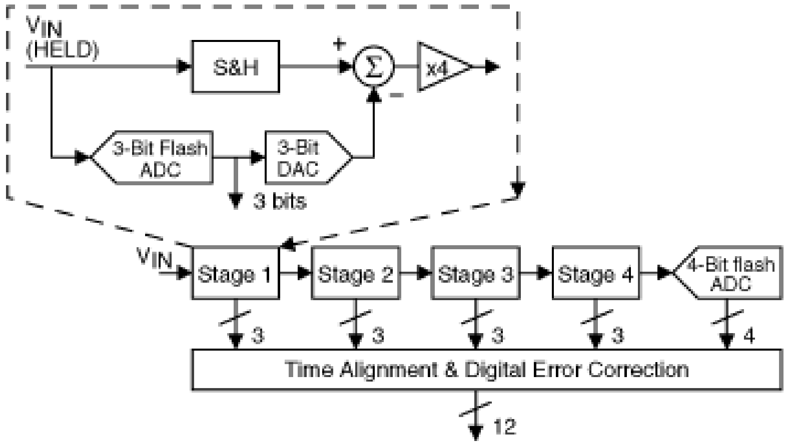


STAGE 1 STAGE 2

Serial/Parallel ADC (pipelined)

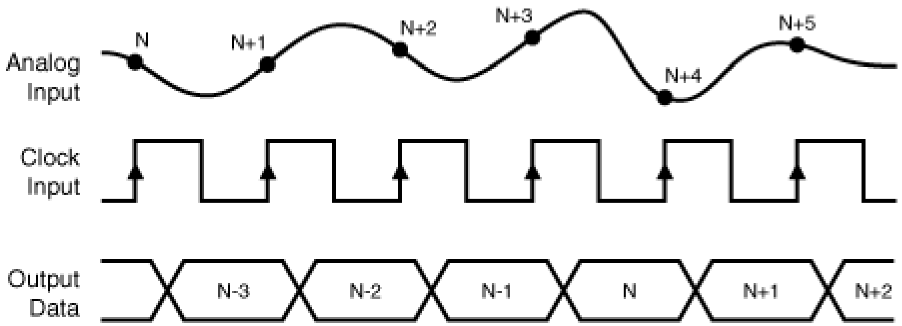
- Example: AD 9220/9221/9223 12 bits pipelined ADC

 - Latency is four cycles;
 - 1 bit overlap between adjacent stages
 - accuracy of ADC in stages 1-4 needs 4 bits; 5-th stage needs greater accuracy;
 - entire ADC accuracy established by 5-th stage



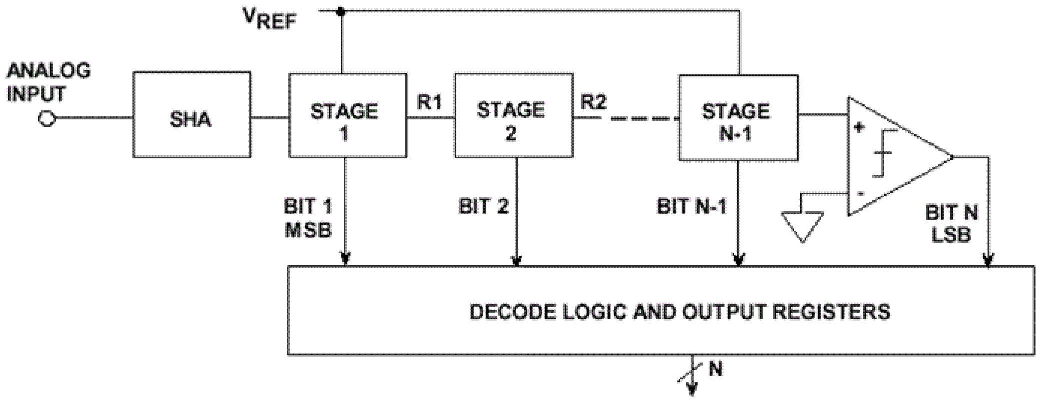
Family Members:

- AD9221 (1.25MSPS), AD9223 (3MSPS), AD9220 (10MSPS)
- Power Dissipation: 60, 100, 250mW, Respectively
- FPBW: 25, 40, 60MHz, Respectively
- Effective Input Noise: 0.1 LSB RMS (Span =5V)
- SINAD: 71 dB
- SFDR: 88dBc
- On-Chip Reference
- Differential Non-Linearity: 0.3 LSB
- Single +5V Supply
- 28-Pin SOIC Package

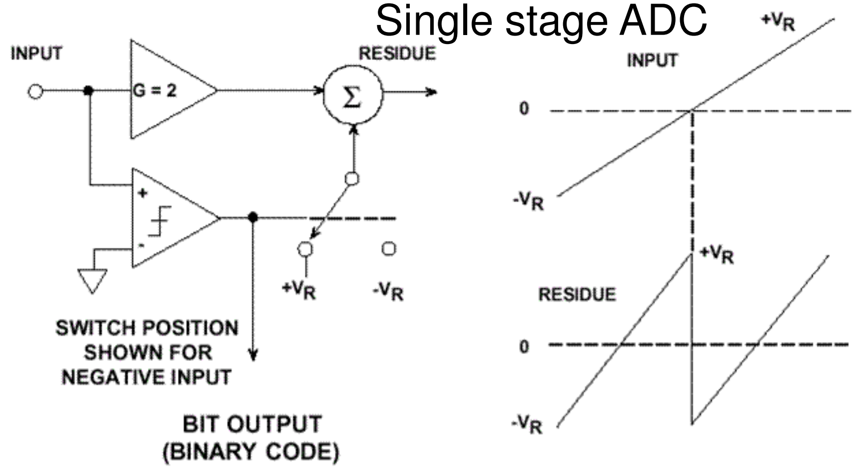


Serial ADC (1 bit per stage)

- it uses the truncating quantization in intermediate stages.
- Example for bipolar case;



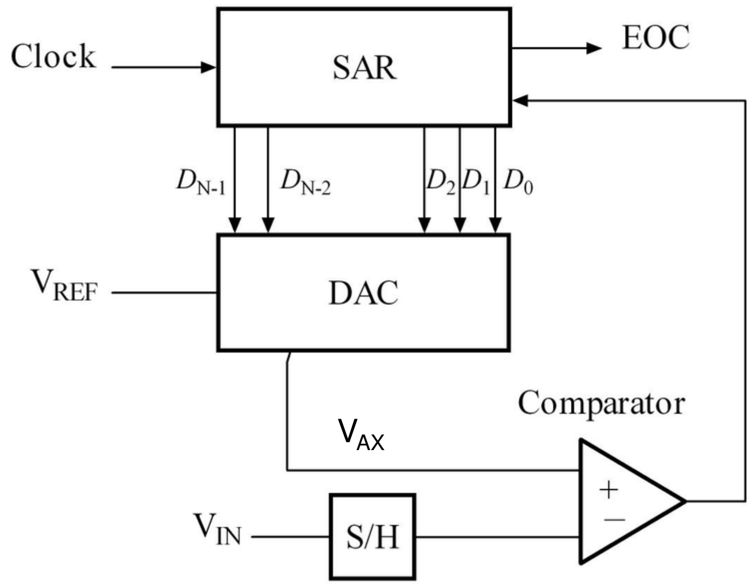
Single stage ADC



Obs: don't confuse with serial output ADC of other technologies (flash, SAR, folded flash, etc)

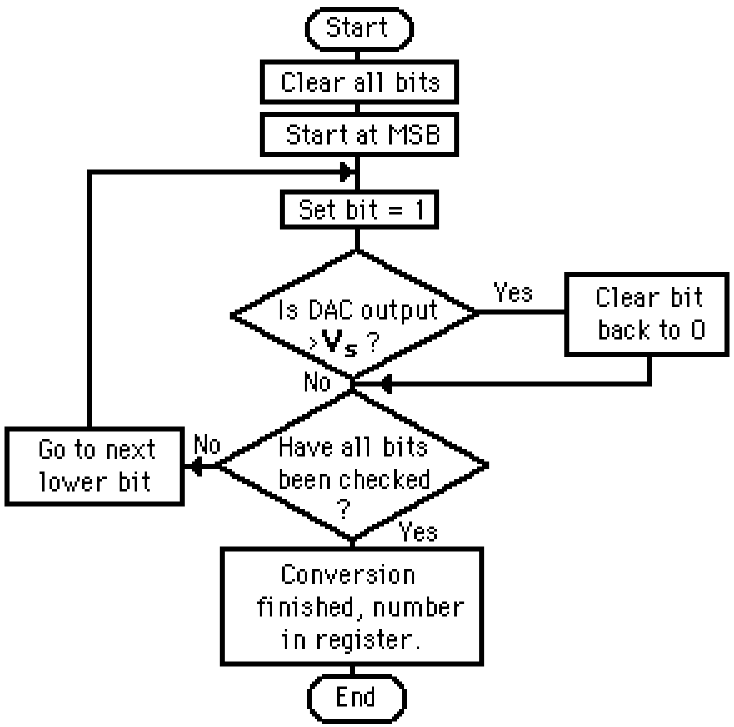
Successive approximation register ADC (SAR)

- SAR = Successive approximation register
- DAC = digital-to-analog converter
- EOC = end of conversion
- SAR = successive approximation register
- S/H = sample and hold circuit
- Vin = input voltage
- Vref = reference voltage



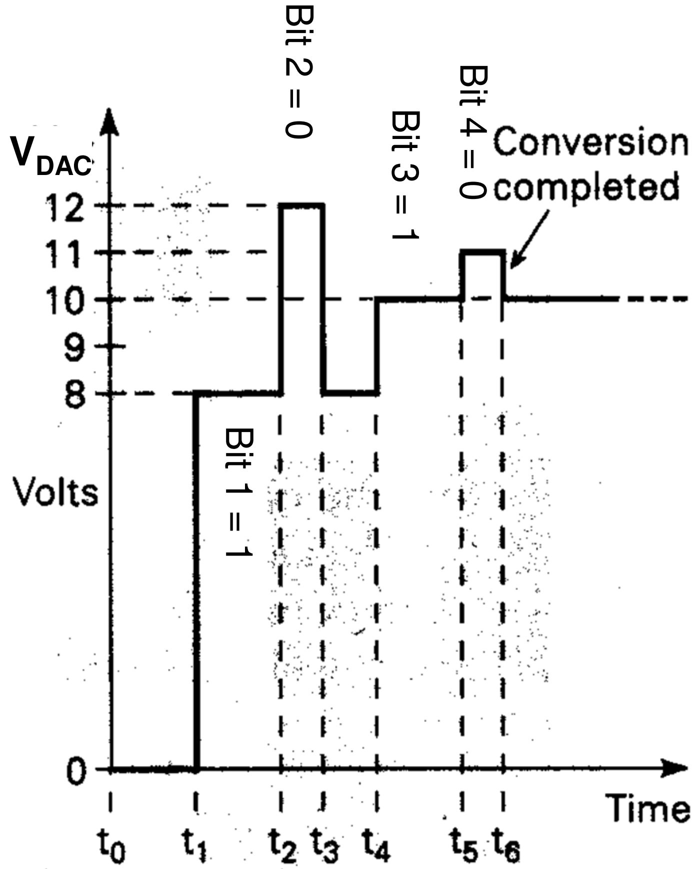
- use a binary search to converge on the closest quantisation level
- Binary search:
  - select middle element
  - If too high select middle element of lower group
  - If too low select middle element of upper group
  - Repeat until 1 element remains
- Constant conversion time (*n* cycles)

Successive approximation algorithm



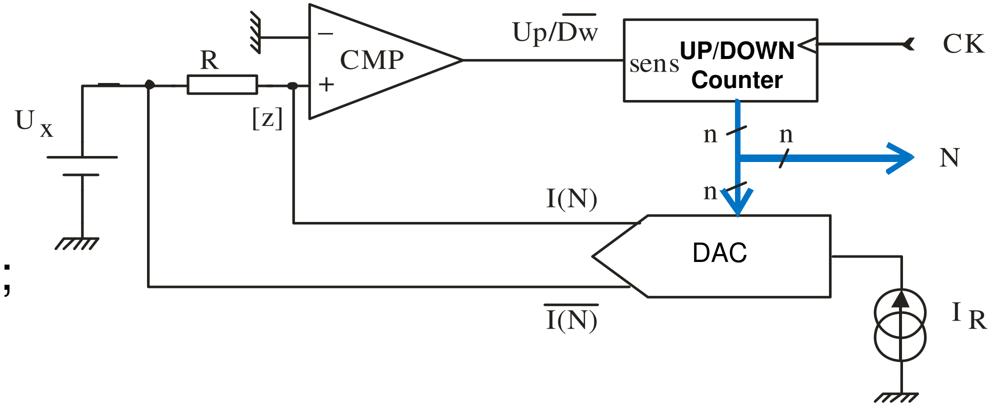
$$T_{conv} = n \cdot T_{CK}$$

Slower than Flash, but far fewer comparators – allows for higher accuracy



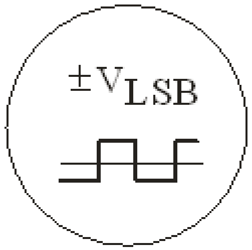
4 Bit SAC

Delta - encoded ADC (tracking ADC)

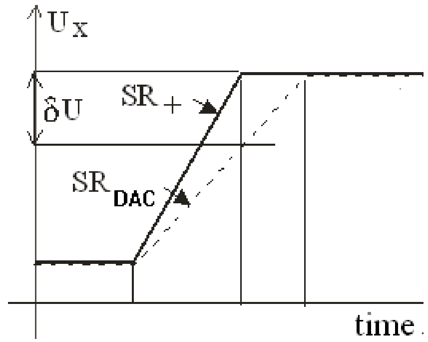


- an up-down counter feeds the DAC;
- CMP compares U_X and DAC output;
- CMP drives U/D counter sens ;
- use a feedback to adjust the counter;
- very wide range and high resolution;
- conversion time is dependent of the input signal level (has a guaranteed value for the worst case);
- introduces *granular noise* for constant and very low frequency signals;
- can expect *overflow error* for rapid variable signal;

Granular noise

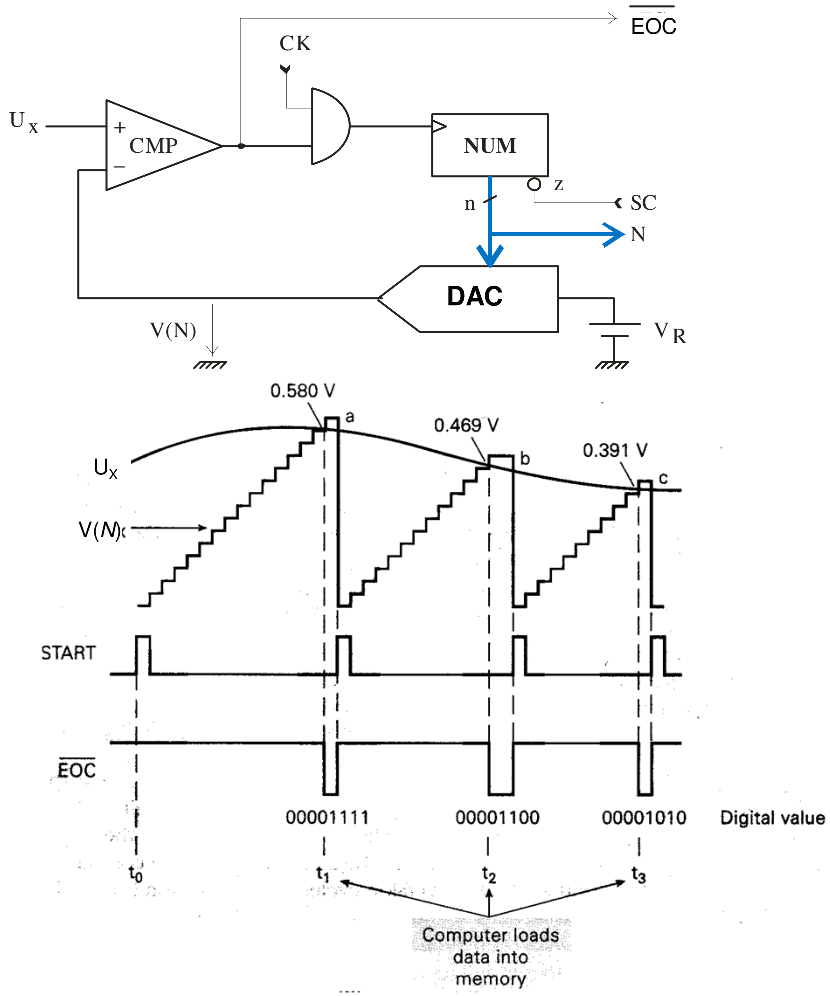


Overflow



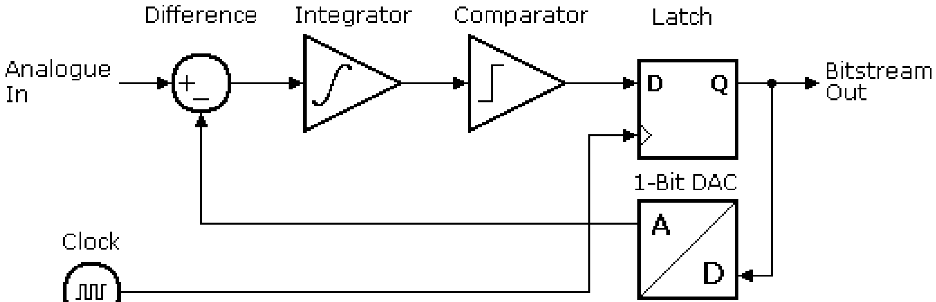
Ramp Compare ADC

- A comparison voltage V(*N*) is ramped up;
- When the comparison voltage matches the sampled voltage (VA) the comparator is triggered – the sampled voltage has been determined;
- Variable Conversion Time (depends when ramp signal matches actual signal):
  - Best case = 1 cycle
  - Worst case = 2^n cycles
- Slower than SAR, same accuracy;

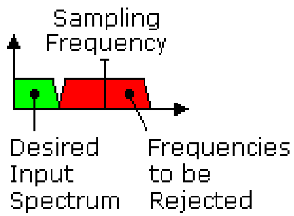


Sigma-delta ADC

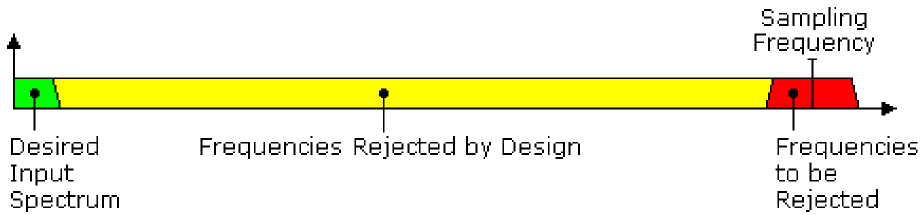
- the output is in the form of a 1 bit serial bit stream;
- analog input variation proportional to the duty of the output digital signal;
- Oversampling (sampling freq 16 – 512 times greater than Nyquist rate);
- low complexity;
- presents "granular" noise for constants and possible overflow error for fast analog input;
- applications: typical low bandwidth digital transmission 22KHz(voice in digital telephone network); recently - ADSL network access, 1-2MHz (multi-bit ADC and multi-bit feedback DAC); digital audio equipment (16-24 bit resolution, 48kS/s);



Sigma-delta ADC of the first order



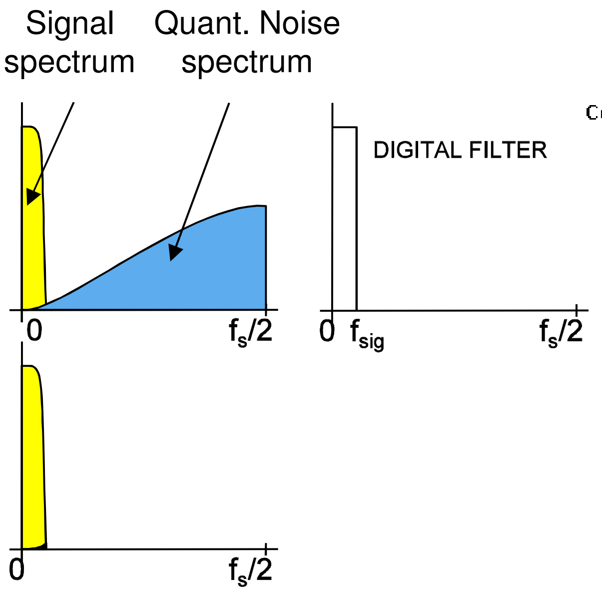
Conventional ADC

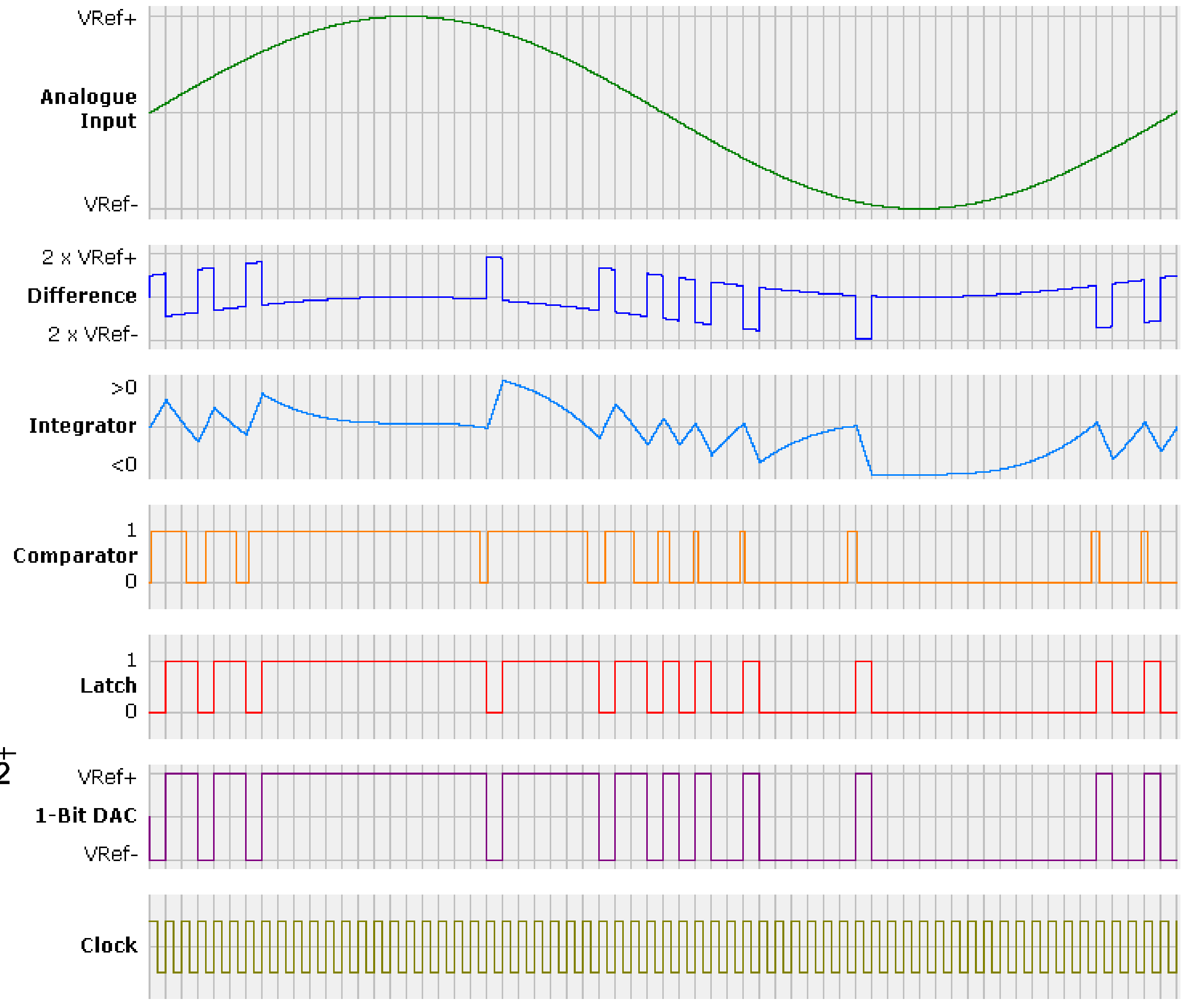


Oversampling ADC (Σ-Δ ADC)

Sigma-delta ADC

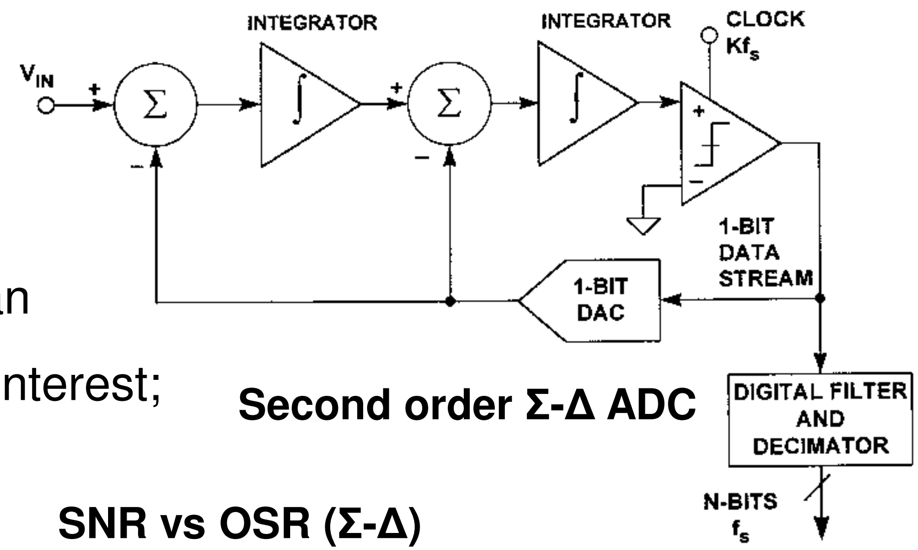
- Quantization noise is pushed out of the signal band;
- digital filter eliminates out of band noise ;
- very high SNR





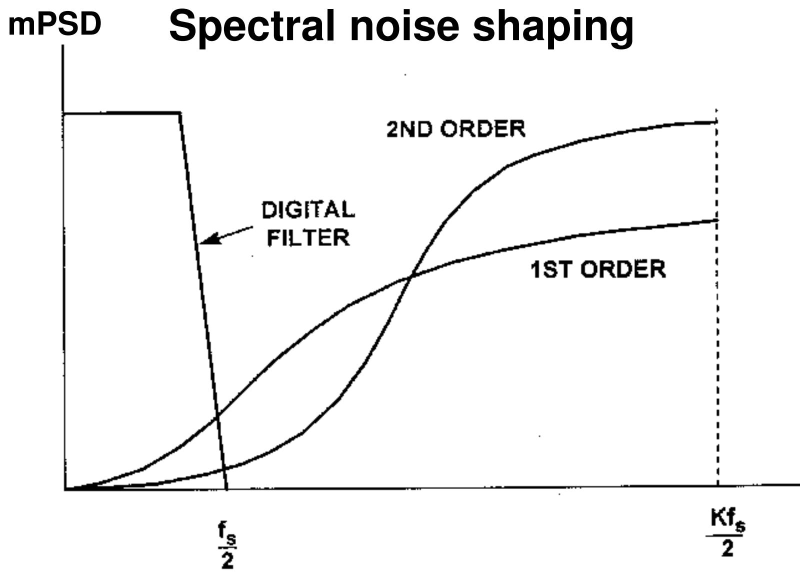
Sigma-delta ADC

- better performances for high order Σ-Δ ADC (second, third, etc.);
- changing LPF (integrator) →BPF we can reduce the noise mDSP (N_0) in band of interest;

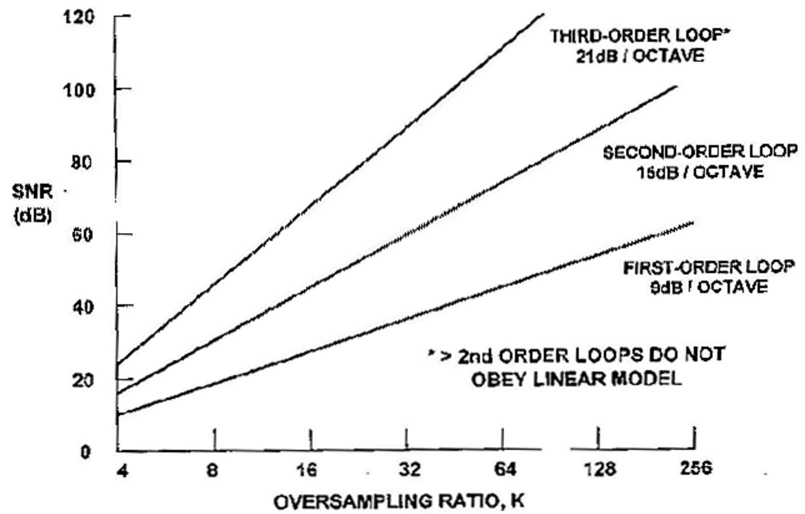


Second order Σ-Δ ADC

Spectral noise shaping



SNR vs OSR (Σ-Δ)



Integrating ADC – single slope

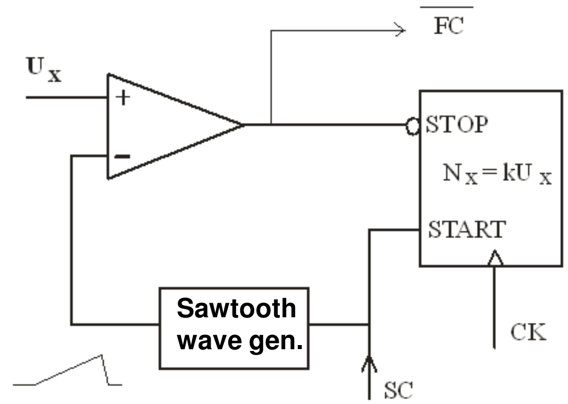
- similar with ramp - compare ADC, but analog devices
- contain: voltage comparator, digital counter, sawtooth wave generator
- Phases:

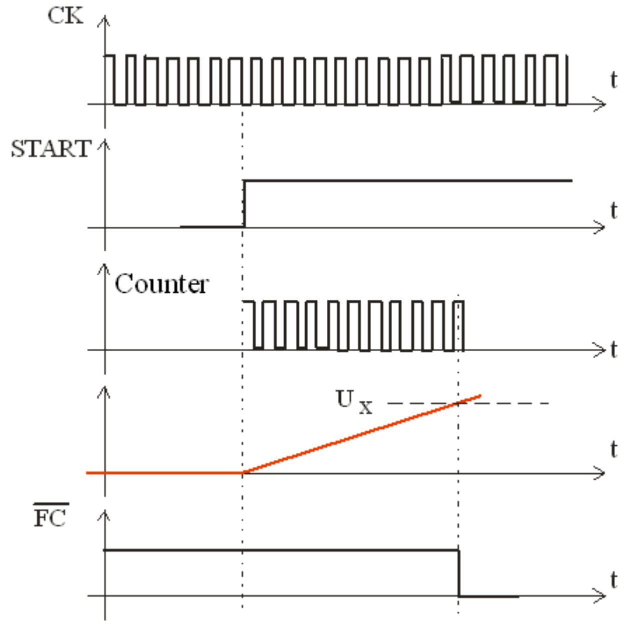
  0. Reset counter and sawtooth wave generator

  1. Start conversion (SC) – start generator and counter

  2. Finish conversion (FC) – When the comparison voltage (analog input) matches the output generator the conversion finish and stop the counter: U_X

$$N_X = k \cdot U_X$$





- Variable Conversion Time (depends when ramp signal matches actual signal):

  - Best case = 1 cycle

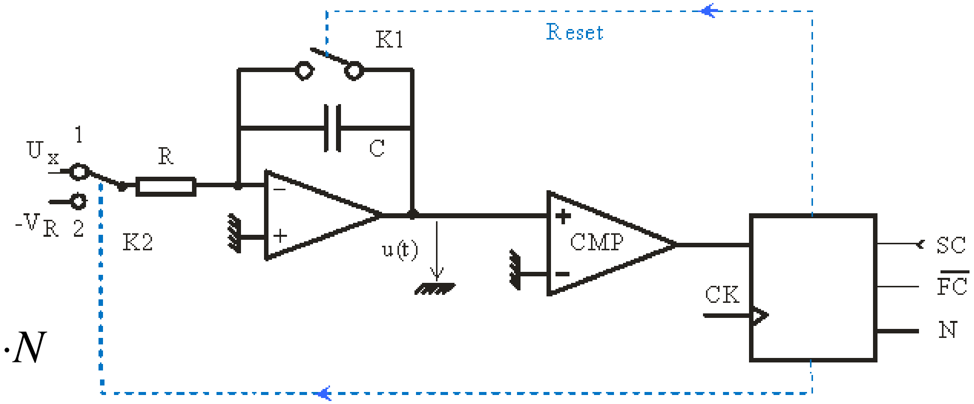
  - Worst case = 2^n cycles

Integrating ADC – dual slope

$$T_1 = 2^n T_{CK} \quad , \quad T_2 = N' \cdot T_{CK}$$

$$\frac{1}{RC}\int_0^{T_1} U_x(t)\mathrm{d}t = \frac{1}{RC}\int_{T_1}^{T_1+t_X} V_\mathrm{R}\mathrm{d}t$$

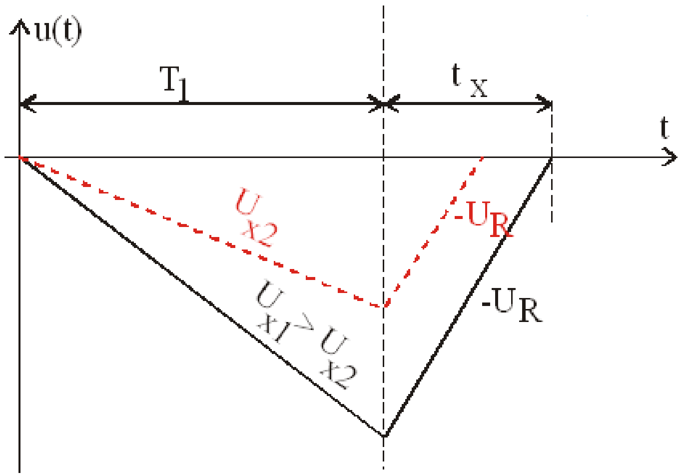
$$\frac{\overline{U_x(t)}}{V_R} = \frac{t_x}{T_1} = \frac{N'}{2^n} \quad \Rightarrow \overline{U_x(t)} = V_R \cdot \sum_{i=1}^{n} b_i 2^{-i} = V_R \cdot N$$



- Absolute values of R and C don't affect operation
- Conversion time is given by:

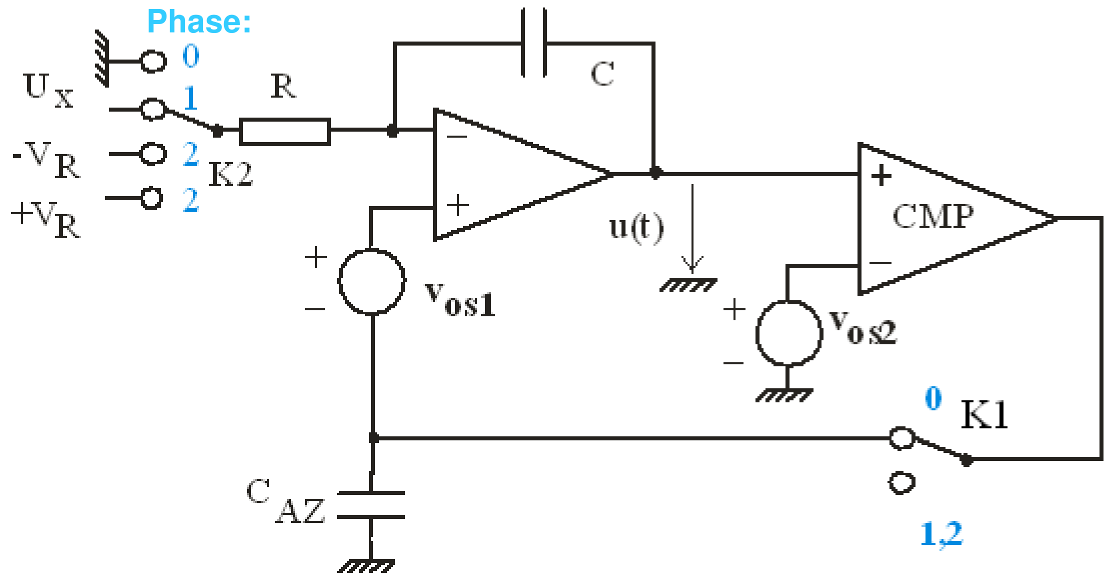
$$T_{conv} = \left(2^n + N'\right)T_{CK} \leq 2^{n+1} T_{CK}$$

- Digital output word gives average value of U_X during first integration phase
- Can be used to get resolutions exceeding 20 bits but at lower conversion rates



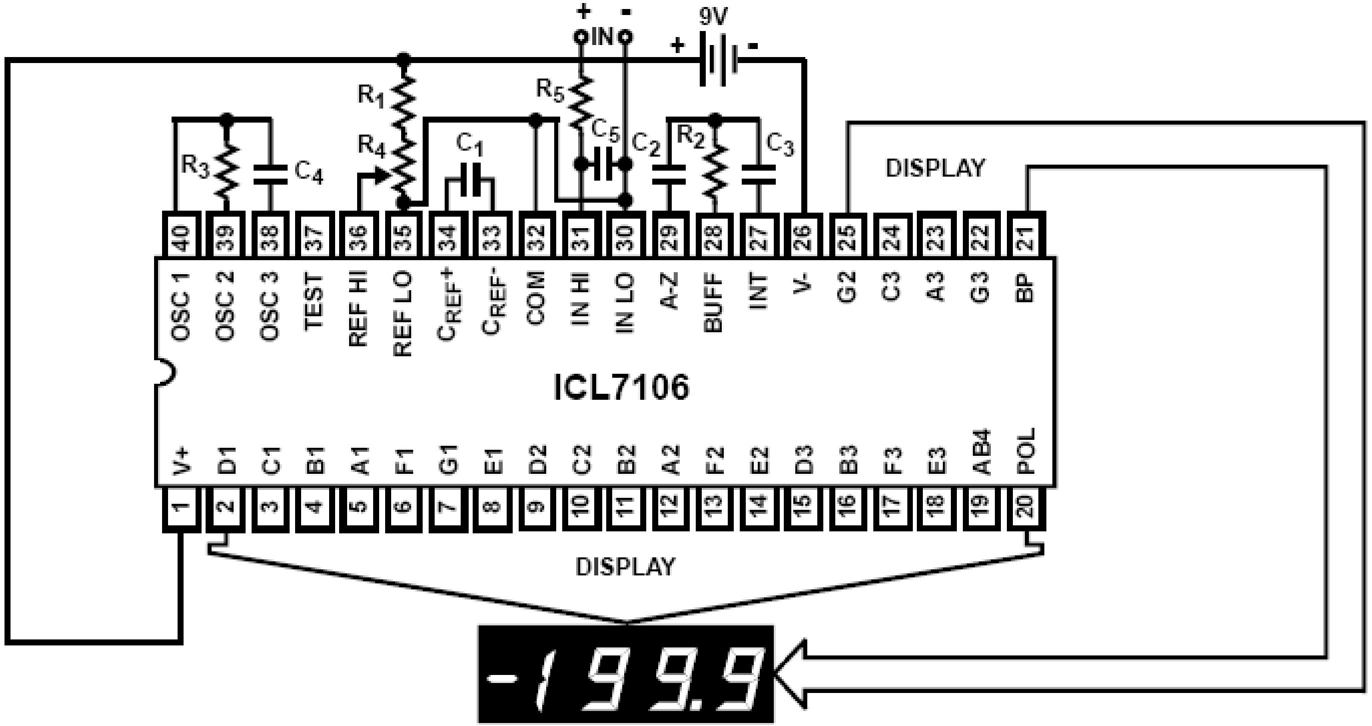
Integrating ADC – dual slope with auto-zero

- Phase 1 – auto zero (K_1=0, K_2=0)
- Phase 2 – unknown voltage integrating (K_1=1, K_2=1)
- Phase 3 - reference voltage integrating (K1=2, K2=2)



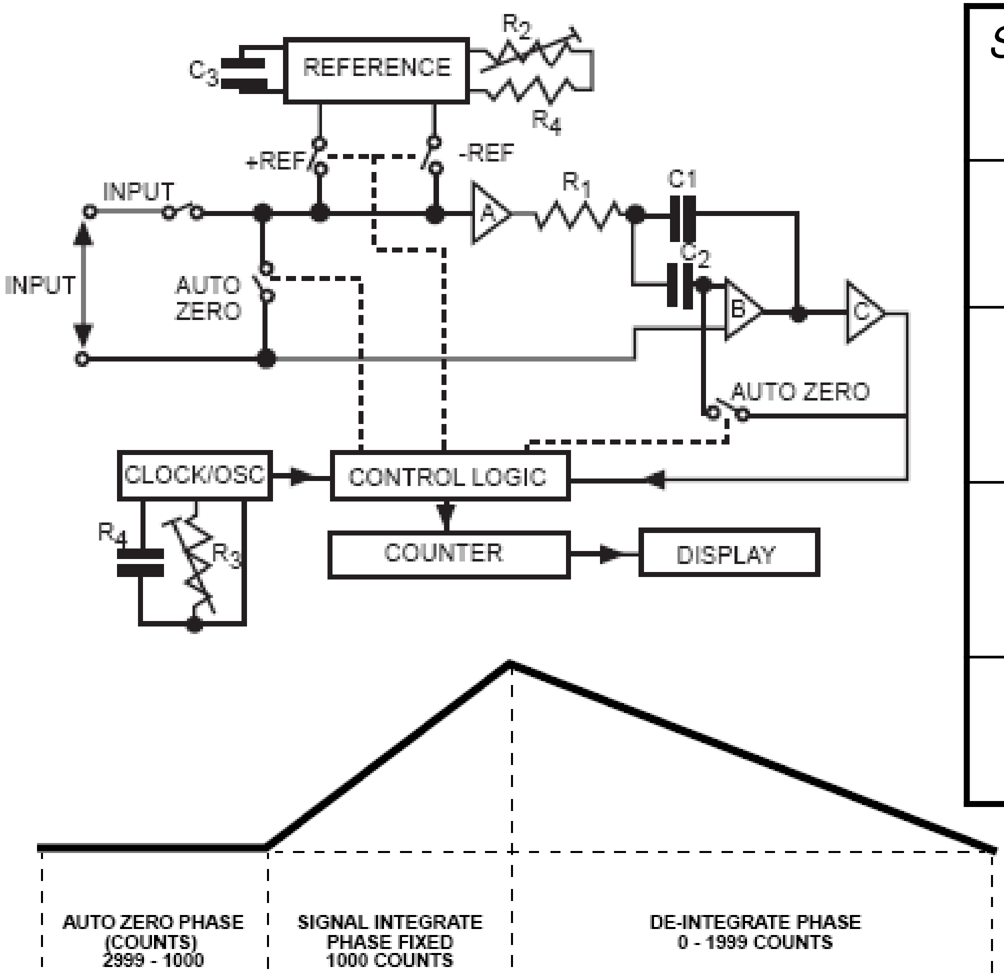
Dual slope ADC application: digital voltmeter

U_x



$C_1 = 0.1\mu F$
$C_2 = 0.47\mu F$
$C_3 = 0.22\mu F$
$C_4 = 100pF$
$C_5 = 0.02\mu F$
$R_1 = 24k\Omega$
$R_2 = 47k\Omega$
$R_3 = 100k\Omega$
$R_4 = 1k\Omega$
$R_5 = 1M\Omega$

Functioning principle – ICL7106



Switches	Phase 0 (AZ)	Phase 1	Phase 2
INPUT	open	close	open
+REF	open	open	funct. of V_{in} sign
-REF	open	open	funct. of V_{in} sign
AUTO-ZERO	close	open	open

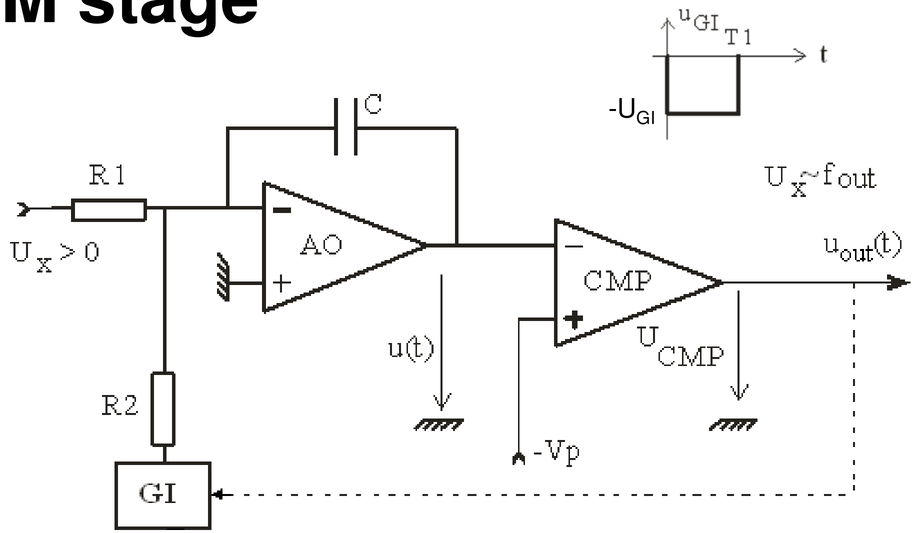
ADC with intermediate FM stage

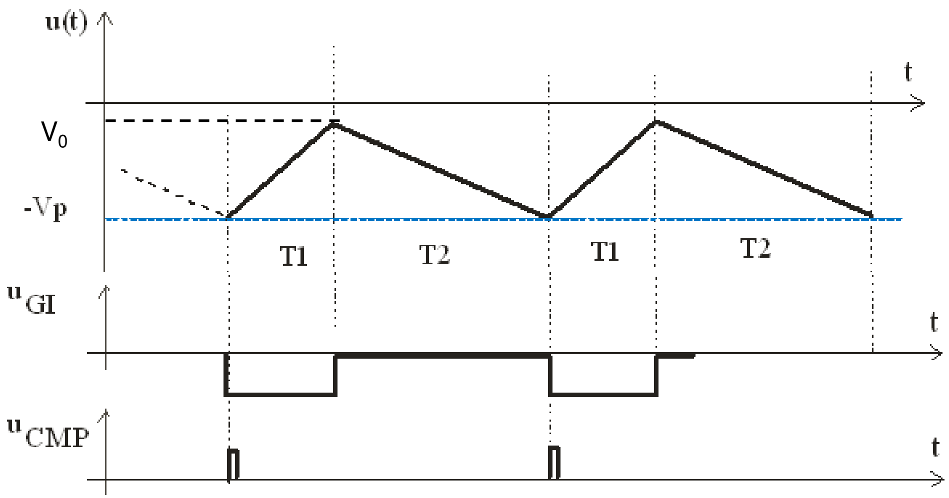
- comprise
  - a voltage-to-frequency converter
  - a frequency counter to convert frequency into a digital count

$$V_P = V_0 - \frac{1}{R_1 C}\int_{T_2} U_x(t)\,dt$$

$$V_0 = V_p + \frac{1}{R_2 C}\int_{T_1} U_{GI}\,dt - \frac{1}{R_1 C}\int_{T_1} U_x(t)\,dt$$

$$\overline{U_x} = \frac{1}{T_1+T_2}\cdot\frac{R_1}{R_2}\cdot U_{GI}\cdot T_1 = K\cdot f_{out}$$

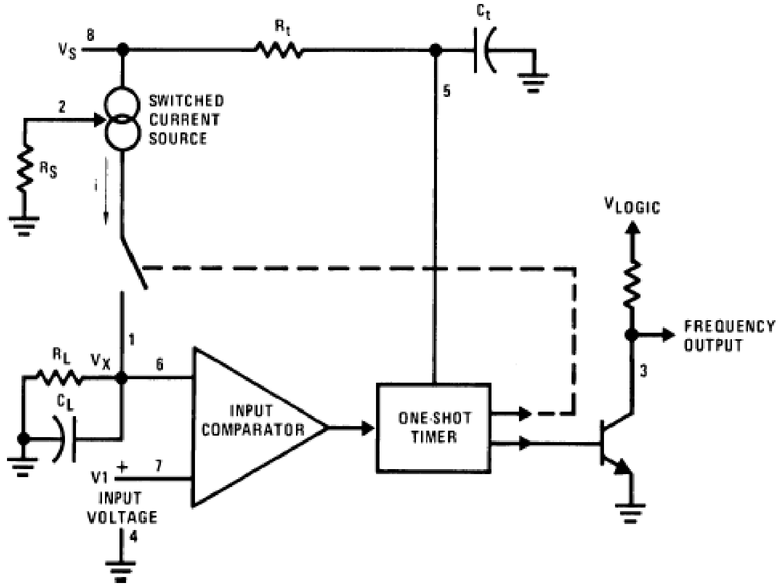




Example U-f converter LM331

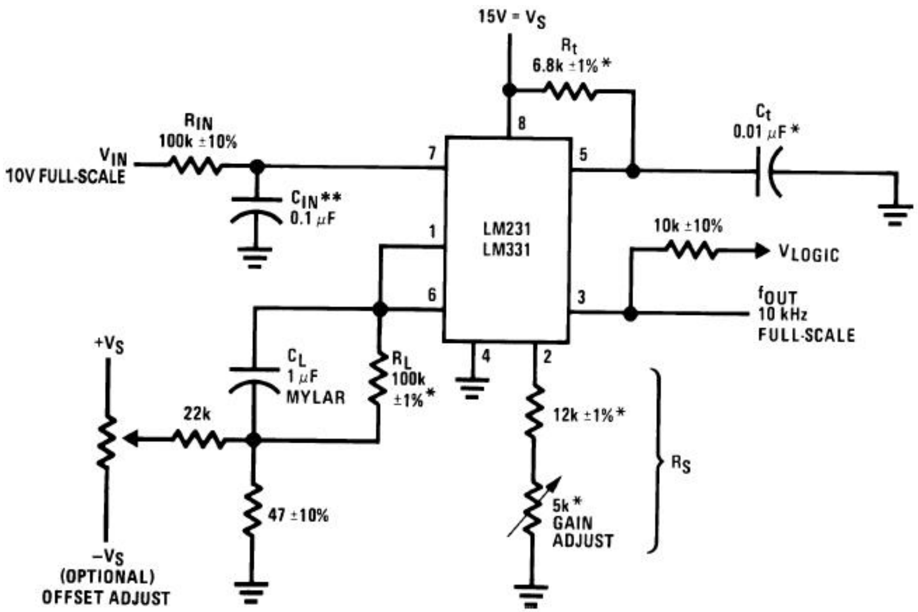
Ux

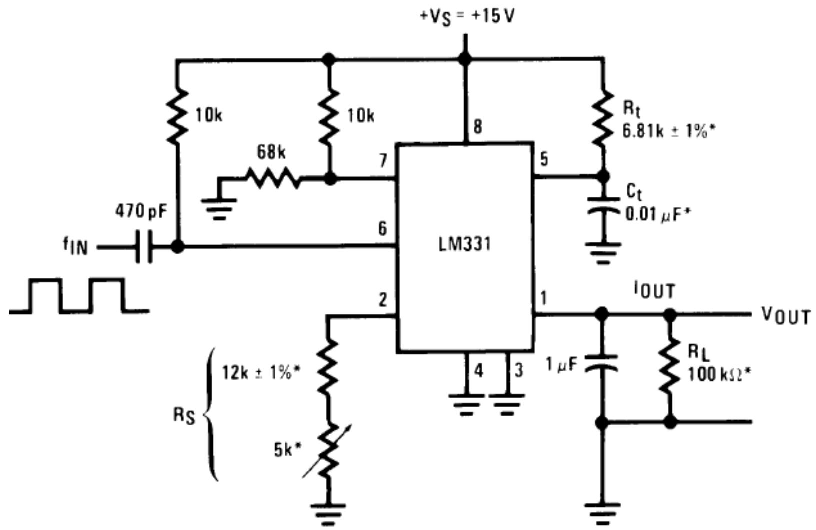
• Longer integration times allow higher resolutions;
• the speed of the converter can be improved by sacrificing resolution;
• few analog devices – high accuracy
• are very popular for low frequency application with remote analog sensor;



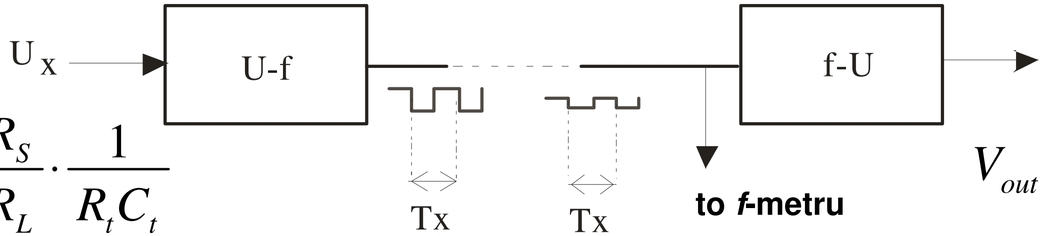
$$f_{out} = \frac{V_{in}}{2.09\text{V}} \cdot \frac{R_S}{R_L} \cdot \frac{1}{R_t C_t}$$

Application. Remote analog voltage measurement with LM331 (National Semiconductor)





Remote transmission



$$f_{out} = \frac{V_{in}}{2.09\text{V}} \cdot \frac{R_S}{R_L} \cdot \frac{1}{R_t C_t}$$

$$V_{out} = f_{in} \cdot 2.09 \cdot \frac{R_L}{R_S} \cdot R_t C_t$$

- ***Ultra-fast* ADC**
  - **Pure electronic ADC: CCD-ADC;**
  - **Optical ADC : Time-stretch ADC.**

• **CCDs - ADC**

Charged-Coupled device (CCD) - sampled analog clocked delay line that memories the input voltage at the clock impulse (analogical memory);

Typically size – 512 stages (samples) and 100MS/s;

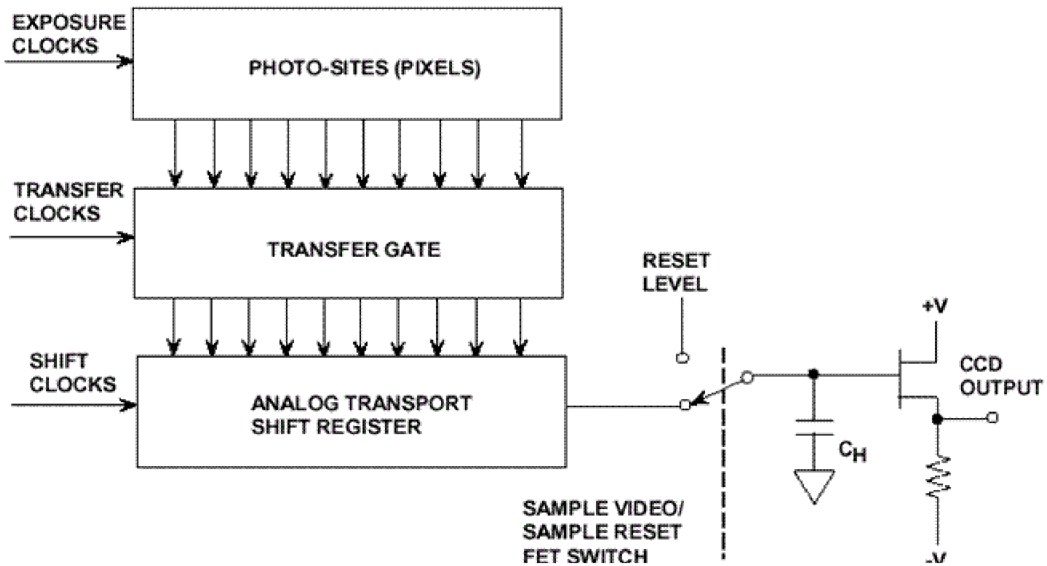
An slower ADC quantizes these analogical values;

For greater effective sample rate (400MS/s) are necessary several CCDs in parallel with staggered clock drive.

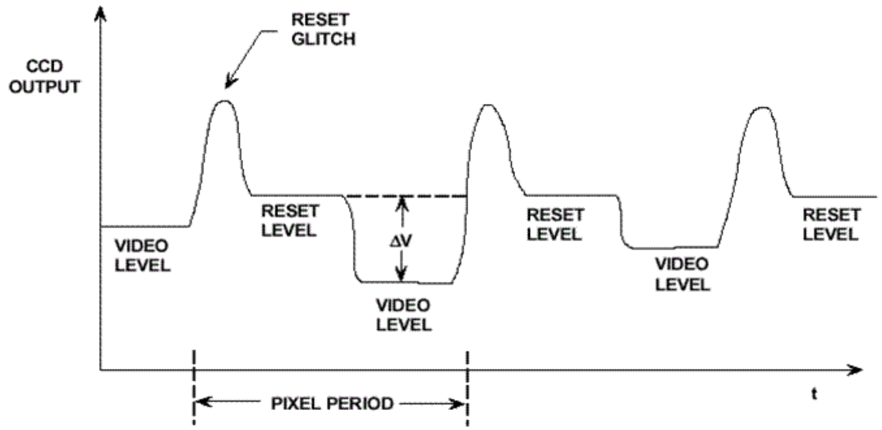
Application – digital video signal capturing

- ***Ultra-fast* ADC**

CCD matrix scheme



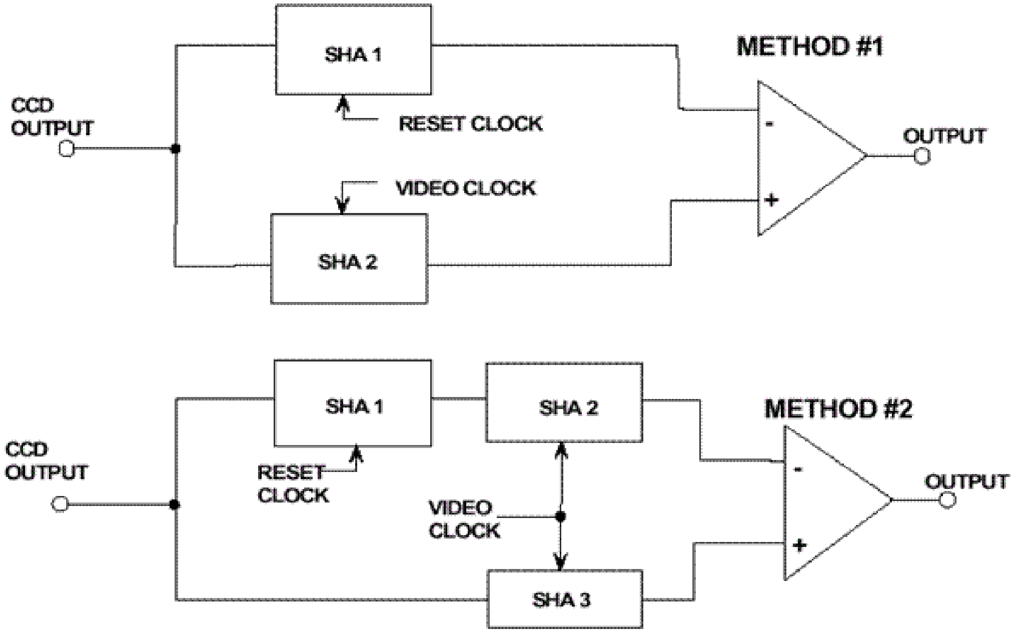
CCD output waveform



Ultra-fast ADC – electronic ADC

- **CCD - ADC**

Correlated double sampling (CDS) minimise switching noise at output



Ultra-fast ADC – optical ADC

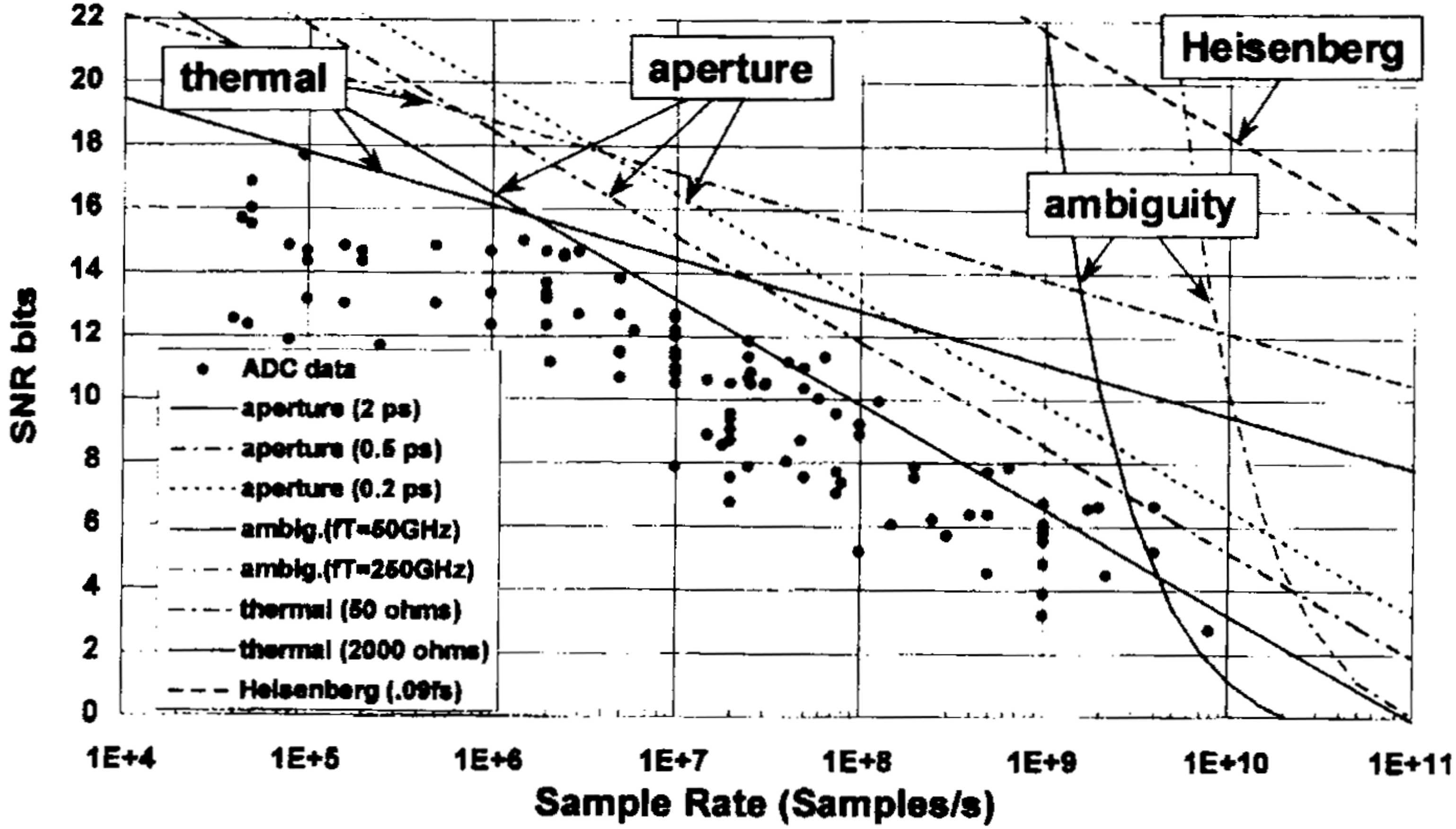
- Electronic (pure) real-time analog-to digital conversion is limited to conversion rates of few GS/s;
- Communication, image processing and radar applications require extremely fast real time A/D conversion;
- A way out of this conversion bottleneck may be the use of photonic concepts for A/D conversion;

Concept for ADC optical conversion:

- Photonic time stretching converter;
- Self-Electro-optic Effect Device based all-optical A/D conversion;
- Optical folding-flash converter;
- Optoelectronic thyristor based photonic smart comparator;

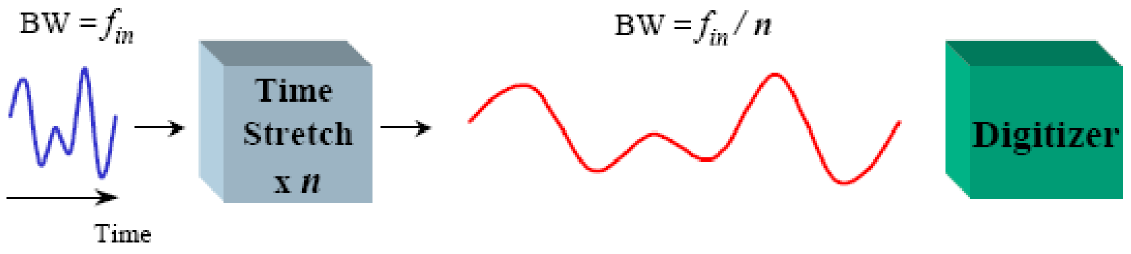
Ultra-fast ADC – optical ADC (cont'd)

Absolute analog to digital conversion rate limits for a required SNR_q



Ultra-fast ADC – optical ADC

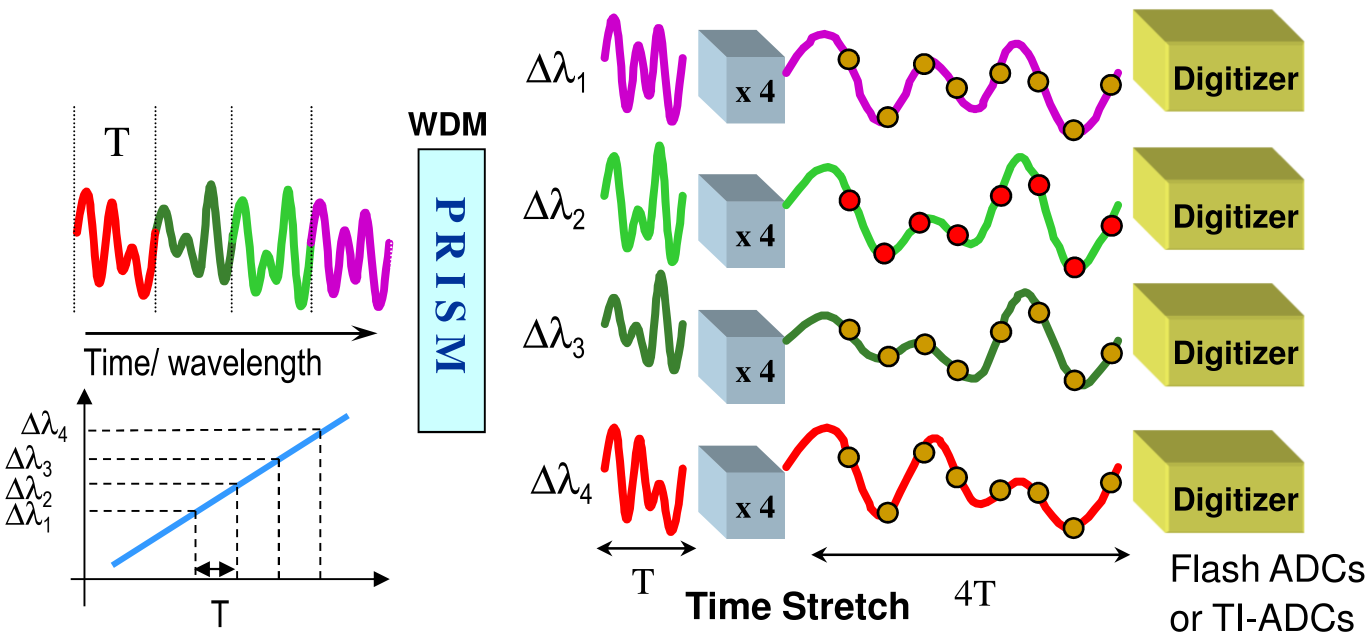
- **Time-stretch ADC (TS-ADC)** Digitizes a very wide bandwidth analog signal by time-stretching the signal prior to digitization using a photonic preprocessor.



- **Improvements:**
  - Effective sampling rate increased by *M ;*
  - Effective Input bandwidth increased by *M ;*
  - Reduce jitter noise ;
  - Eliminates the need for samples interleaving ;
  - Ideal for time-limited signals or fast time-varying signals ;

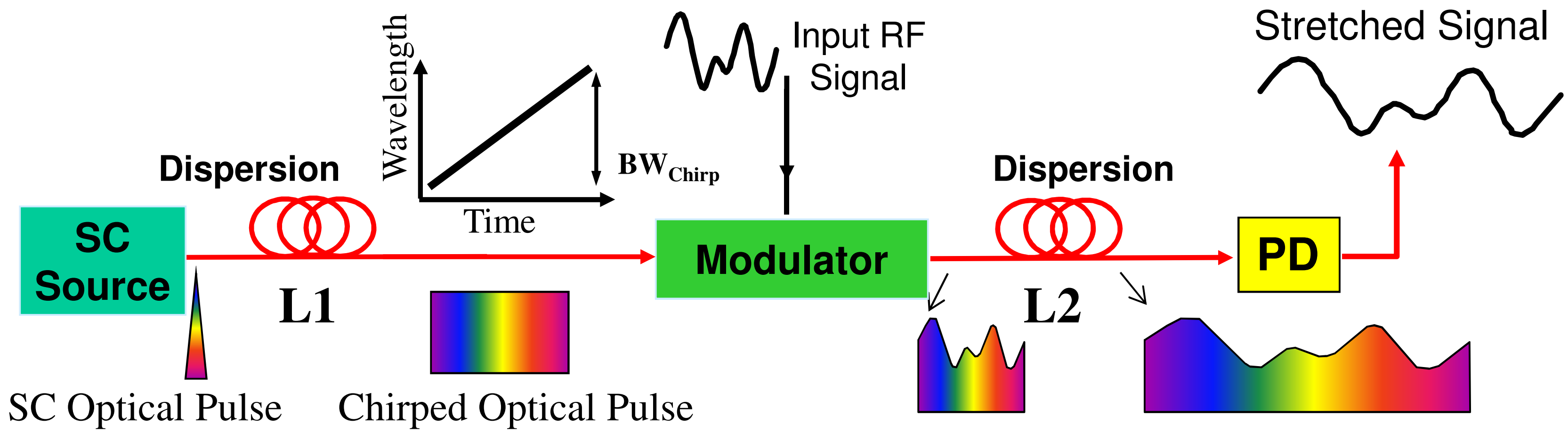
Ultra-fast ADC – optical ADC (cont'd)

- **Schematic photonic preprocessor for time-stretching**
  - Each ADC see the slowed-down signal;
  - Full Nyquist sampling by each ADC;
  - By allowing for finite overlap between segments, mismatch error can be estimated from the signal itself;



Ultra-fast ADC – optical ADC (cont'd)

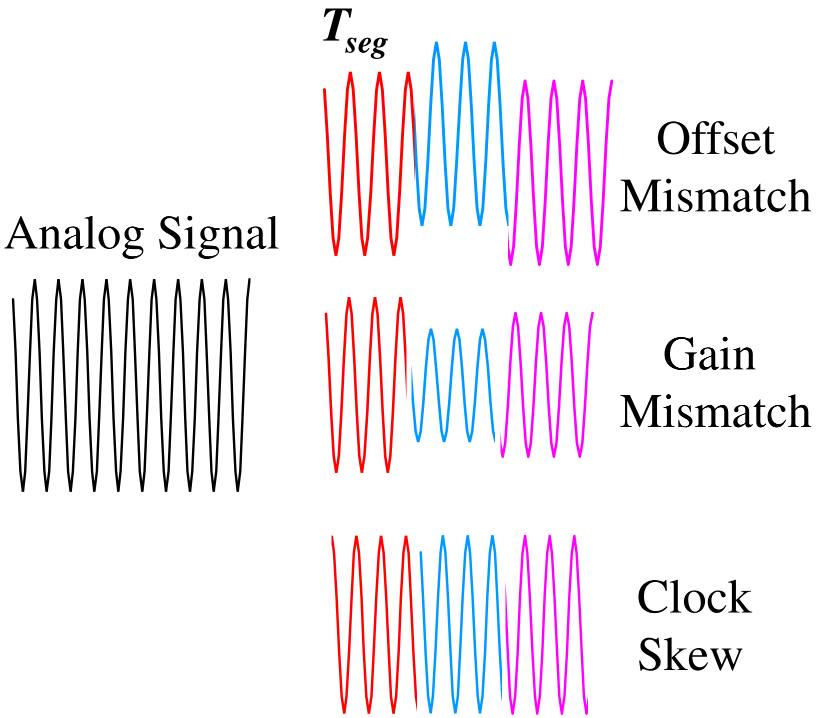
Photonic Time Stretch System



Stretch Factor = 1 + L_2 / L_1
Time Aperture = $D \times \Delta\lambda \times L_1$
Baseband BW* = $\sqrt{1/(8\pi\beta_2 L_1)}$
Time BW Product* = $\Delta f_{op} / 2\Delta f_{RF}$

Ultra-fast ADC – optical ADC (cont'd)

Mismatches in TS-ADC Arrays



$$S(\omega)=\frac{2\pi}{T_s}\sum_{k=0}^{L-1}F_k\times\delta\left(\omega-\frac{k\omega_s}{L}\right)$$

$$F_k=\frac{1}{L}\left[\sum_{m=0}^{M-1}b_m\exp\left(-j\frac{2\pi km}{M}\right)\right]\times\frac{\sin\frac{\pi kN}{L}}{\sin\frac{\pi k}{L}}\cdot\exp\left[-j\frac{\pi k(N-1)}{L}\right]$$

$$S(\omega)=\frac{2\pi}{T_s}\sum_{k=0}^{L-1}F_k\times\delta\left(\omega-\omega_o-\frac{k\omega_s}{L}\right)$$

$$S(\omega)=\frac{1}{T_s}\sum_{k=-\infty}^{\infty}F_k\times\delta\left(\omega-\omega_0-\frac{k\omega_s}{L}\right)$$

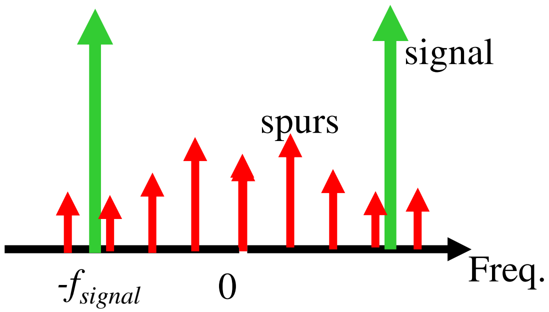
$$F_k=\frac{1}{L}\left[\sum_{m=0}^{M-1}\exp(-j\omega_0 r_m T_s)\exp\left(-j\frac{2\pi km}{M}\right)\right]\times\frac{\sin\frac{\pi kN}{L}}{\sin\frac{\pi k}{L}}\times\exp\left[-j\frac{\pi k(N-1)}{L}\right]$$

L=MxN: the period of distortion pattern

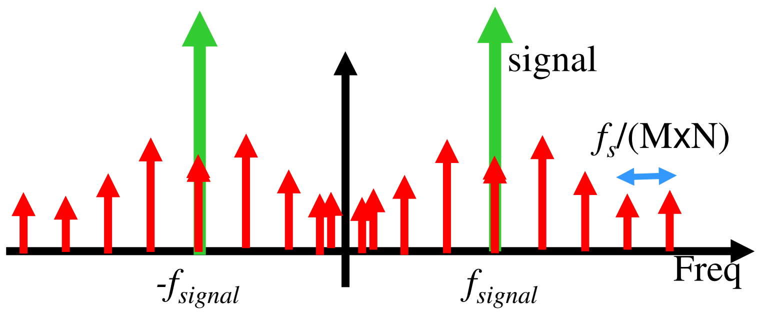
■ *Ultra-fast* ADC – optical ADC (cont'd)

❑ Mismatches in TS-ADC Arrays – Spectrum

Offset Error
Spurs at harmonics of
f_{signal}/(MxN)

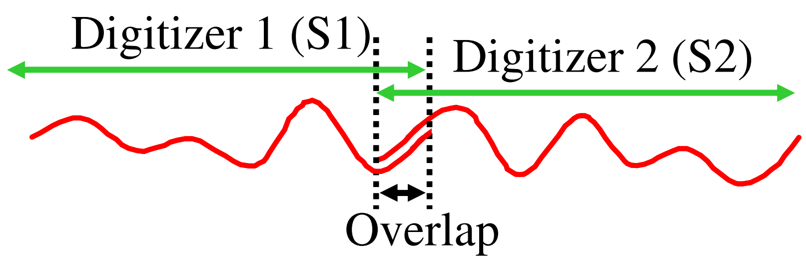


Gain Error or Clock Skew
Sidebands at multiples of
f_{signal}/(MxN) centered at f_{signal}



❑ Overlap between segments

Slight redundancy in sampling could (time overlaping) significantly improve the ADC performance;



Ultra-fast ADC – optical ADC (cont'd)

•Time-stretch ADC (TS-ADC)

- ADC SFDR Improvements

	RMSE (before)	SFDR (before)	RMSE (after)	SFDR (after)
Offset	4%	-36dBc	0.3%	-58dBc
Gain	4%	-36dBc	0.35%	-57dBc
Clock Skew	8%	-26dBc	0.45%	-51dBc

- **Conclusions:**
  - Signal is reconstructed based on segments, instead of the individual samples;
  - In each segment, the sampling is above the Nyquist sampling rate;
  - Subject to the similar mismatch as the sample-interleaved counterpart;

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