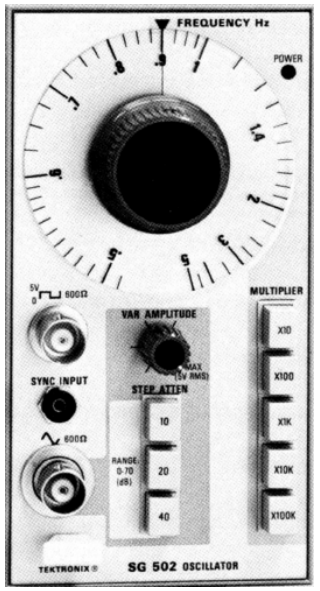
Signal Generator & Function generator

Signal source

• **signal generator** – generates sine wave and optionally few others signal wave form : square (η=50%), saw tooth, triangle (from original sin wave);
  • advantage: low THD for sine wave
  • disadvantage: limitation in other waveform generation;
• **function generator** – generates basically other waveform: square (variable η), triangle, etc.
  • **Direct analog synthesizer** generator (DAS) - Sine wave is obtained indirectly from triangle wave with sine shape circuit (analog generator);
  • **Direct digital synthesizer** generator (DDS) – the wave form is obtained by DAC conversion of signal digital samples;
  • advantage: many waveforms with variables parameters
  • disadvantage: significant THD for sine wave; limited high frequency signals (DDS)

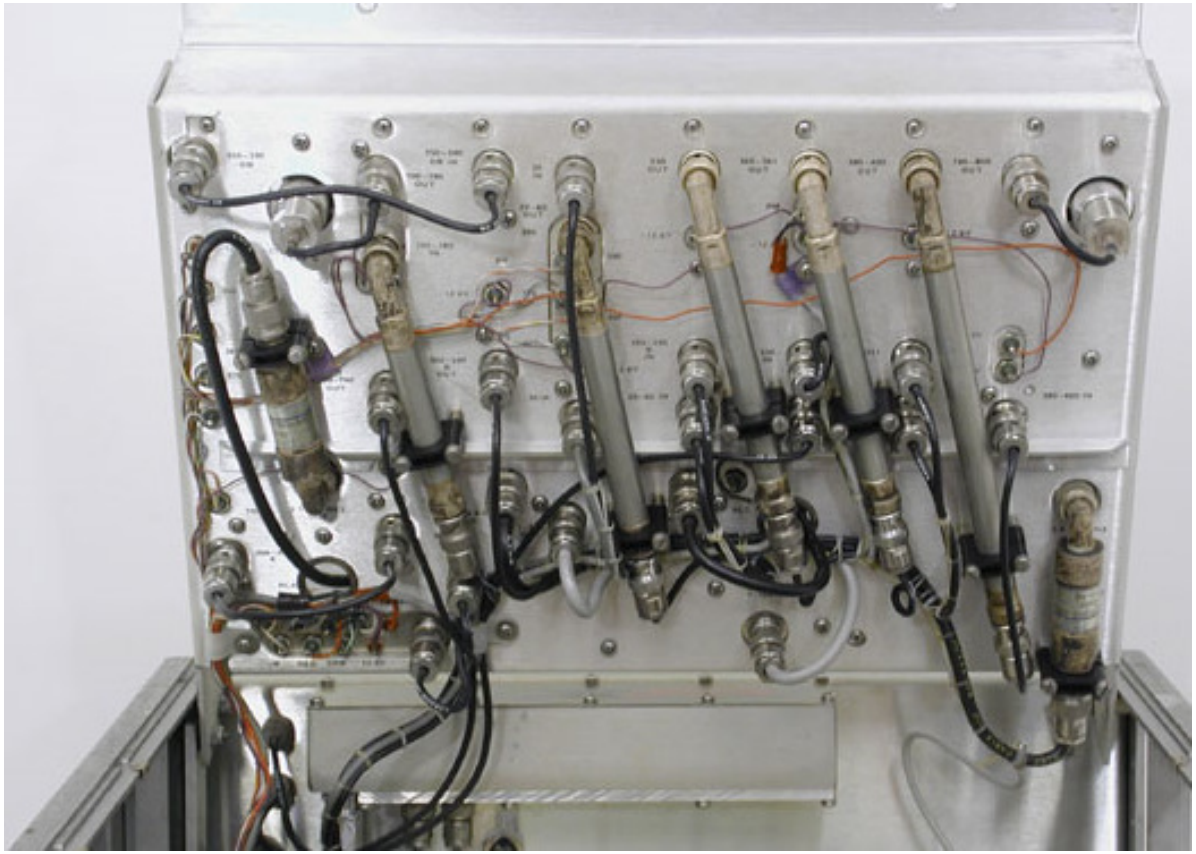
Analog Signal source



- **RC oscillator signal generator**
  - Low complexity (RC oscillator);
  - Very low TDH for sine wave;
  - Poor frequency stability and resolution;
  - Small frequency range (<500kHz)

- **Direct analog synthesizer (DAS)**
  - High frequency stability (0.003ppm/ 24h)
  - Good frequency resolution (Δf=0.01Hz)
  - Large frequency range (0.1 – 500MHz)
  - Very high complexity and difficult adjustments (uses one quartz crystal and analog multipliers for frequency synthesis)

- **DAS Example – HP5100**

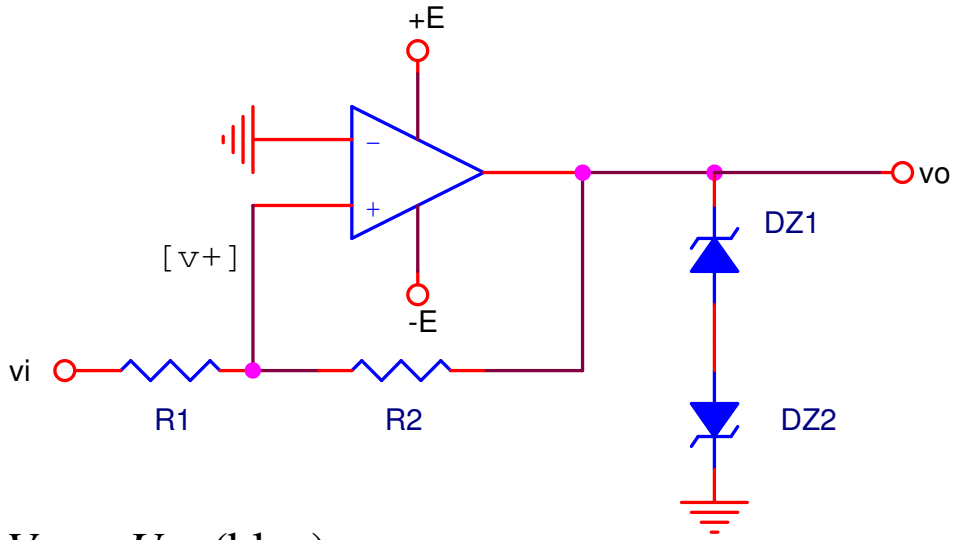


Low frequency function generators

• generate square waveform, triangle waveform (using RC integrator circuit), sine wave (conversion from triangle);
• advantages/disadvantages
    • low complexity;
    • AM modulation and other waveform generation possibility;
    • small frequency range (mHz – 1 MHz);
    • acceptable stability and frequency resolution;
    • poor THD for sine wave;

Hystheresis comparator

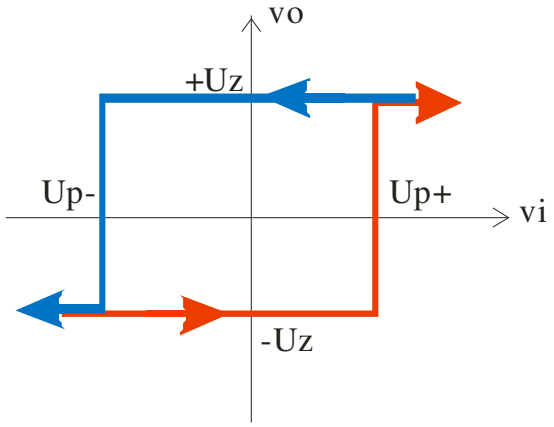
- component of oscillator



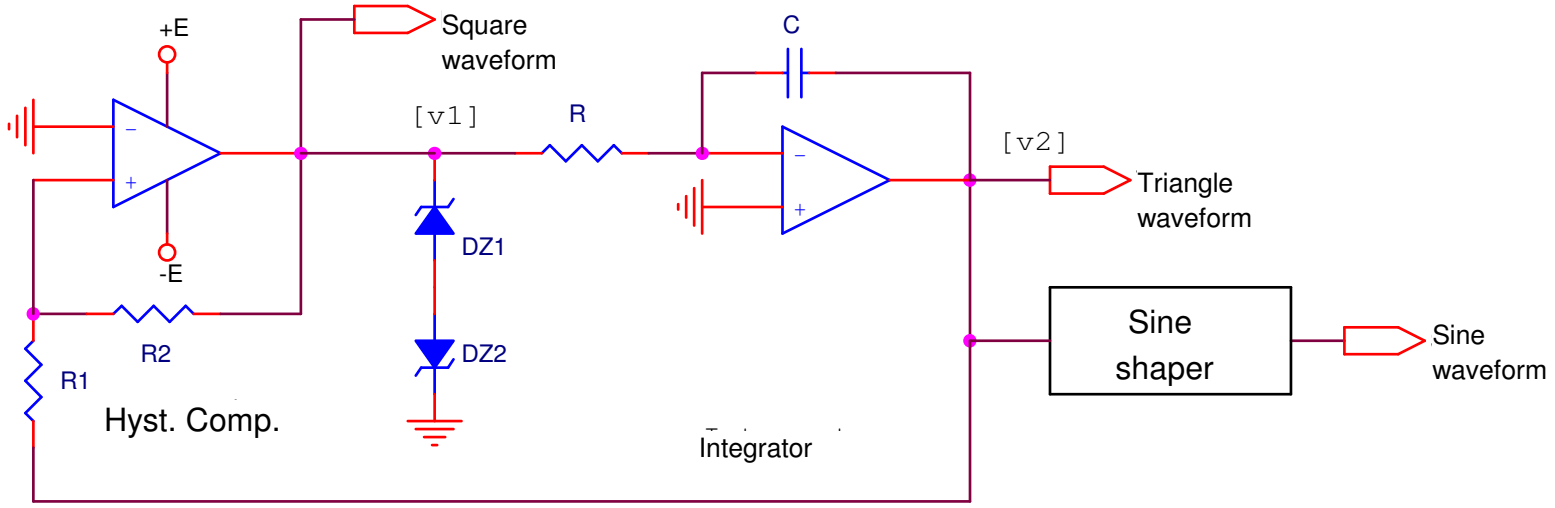
$$V_0 = +U_Z \;,\; v_i \downarrow \;,\; v_i < U_{P-} = -\frac{R_1}{R_2}U_Z \Rightarrow V_0 = -U_Z \quad \text{(blue)}$$

$$V_0 = -U_Z \;,\; v_i \uparrow \;,\; v_i > U_{P+} = \frac{R_1}{R_2}U_Z \Rightarrow V_0 = +U_Z \quad \text{(red)}$$

$$\Delta U_P = U_{P+} - U_{P-} = \frac{2R_1}{R_2}U_Z \quad \text{(trigger window)}$$



Low frequency function generator

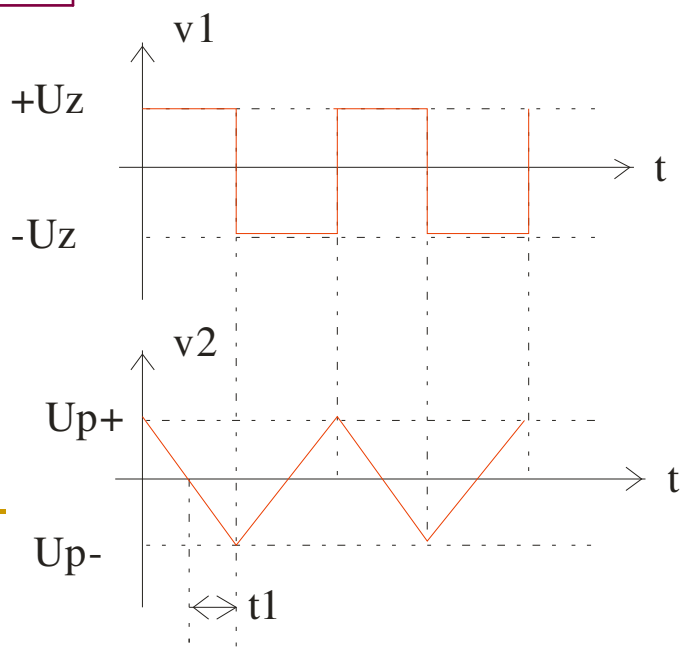


t=0 , $v_1=+U_z$, $v_2=U_{P+}$ decreases

$t_1=RCR_1/R_2$, $T=4t_1$

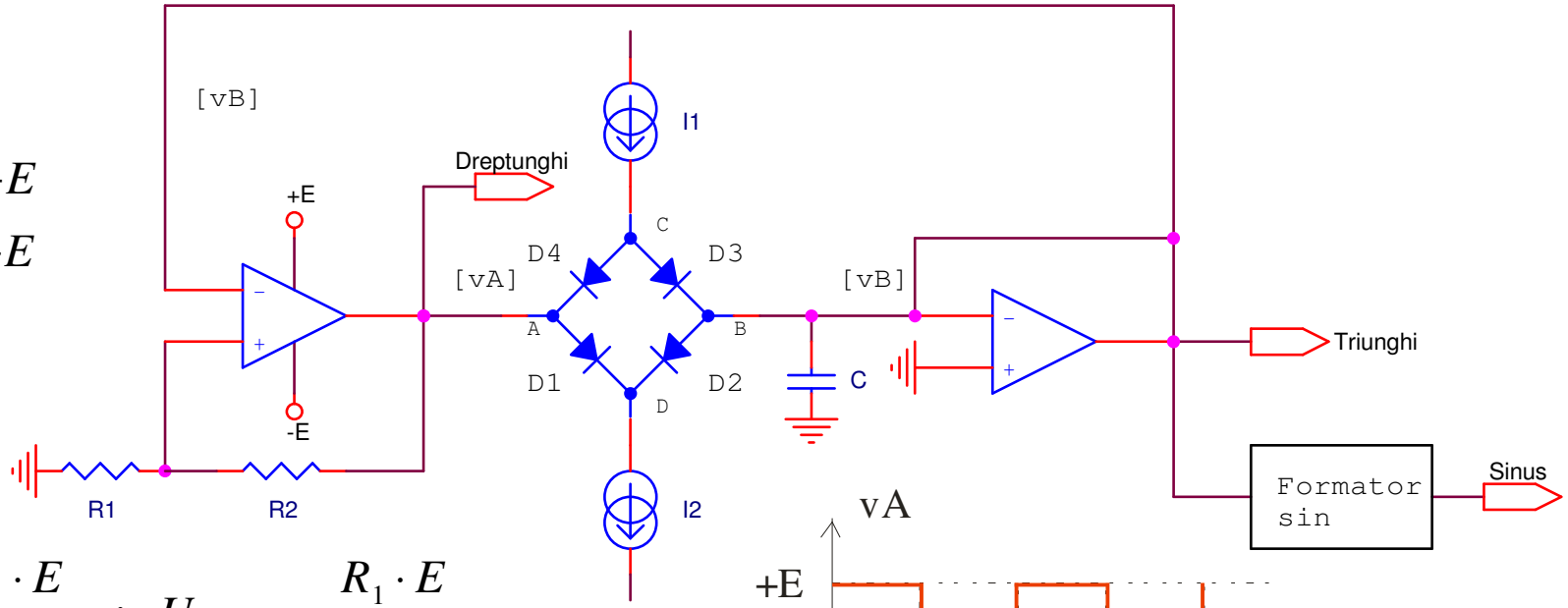
Note: $R_1=R_2 \rightarrow U_p=U_Z$

advantage: same amplitude for square and triangle waveform



Low-medium frequency function generator

$$\begin{cases} +U_Z = +E \\ -U_Z = -E \end{cases}$$

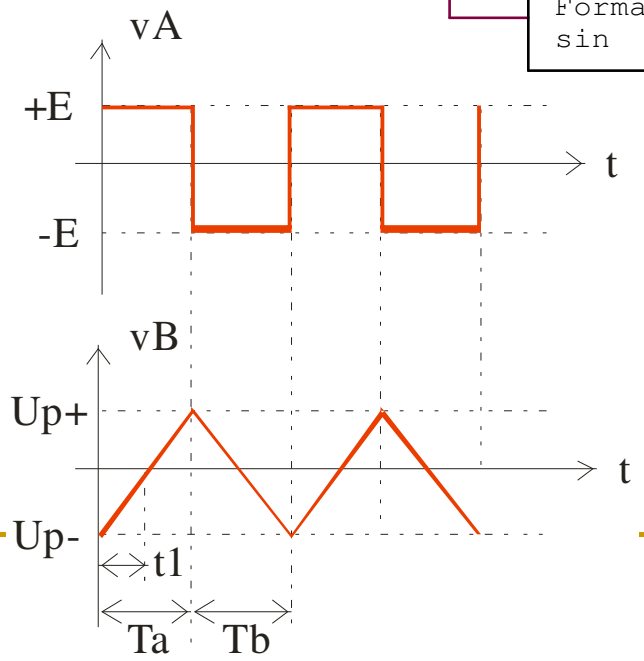


$$U_{P+} = \frac{R_1 \cdot E}{R_1 + R_2} \quad ; \quad U_{P-} = -\frac{R_1 \cdot E}{R_1 + R_2}$$

$$v_A = +E \Rightarrow \text{cmd } I_1 \left(D_{1,3} \text{ on}, D_{2,4} \text{ off} \right)$$

$$v_A = -E \Rightarrow \text{cmd } I_2 \left(D_{1,3} \text{ off}, D_{2,4} \text{ on} \right)$$

$$T = T_a + T_b = 2U_P C \left(\frac{1}{I_1} + \frac{1}{I_2} \right)$$



Low-medium frequency function generator

- adjustable duty factor scheme

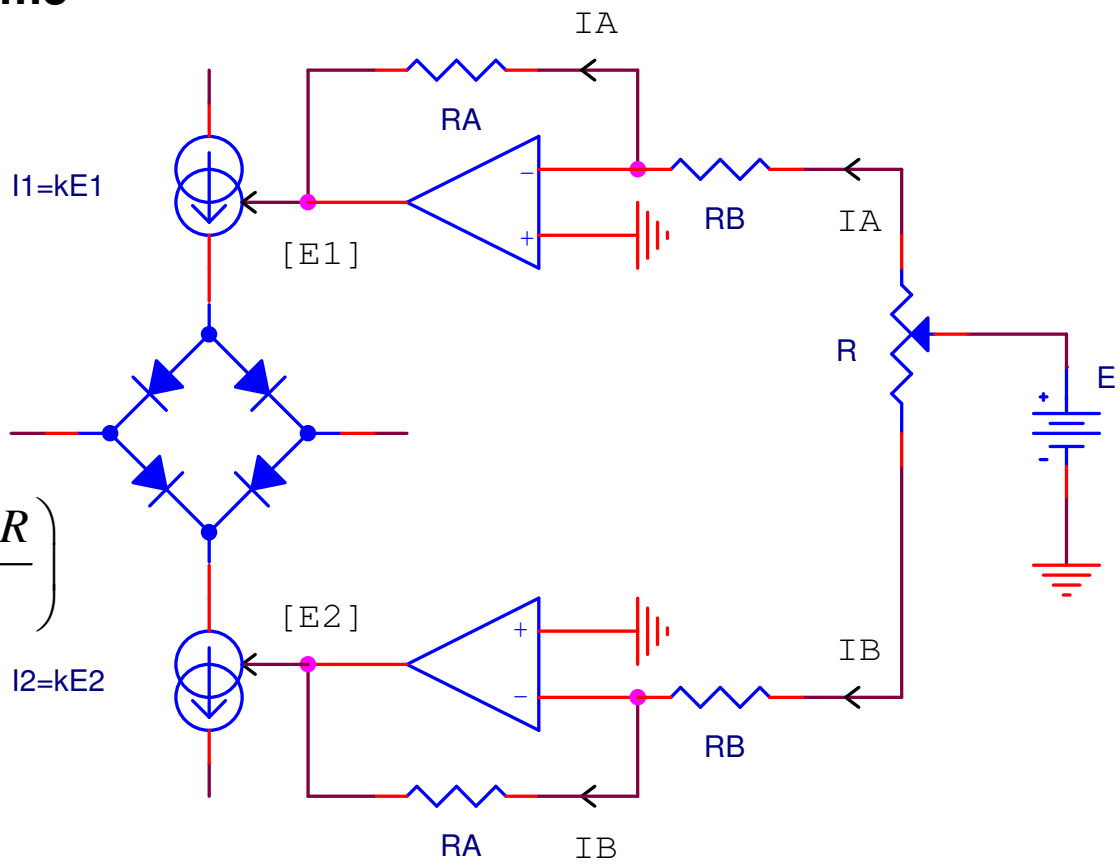
$$T_a = \frac{2U_P C}{I_1} = \frac{2U_P C}{kR_A E}\left(R_B + \alpha R\right)$$

$$T = T_a + T_b = 2U_P C\left(\frac{1}{I_1} + \frac{1}{I_2}\right) =$$

$$= 2U_P C\left(\frac{R_B + \alpha R}{kR_A E} + \frac{R_B + (1-\alpha)R}{kR_A E}\right)$$

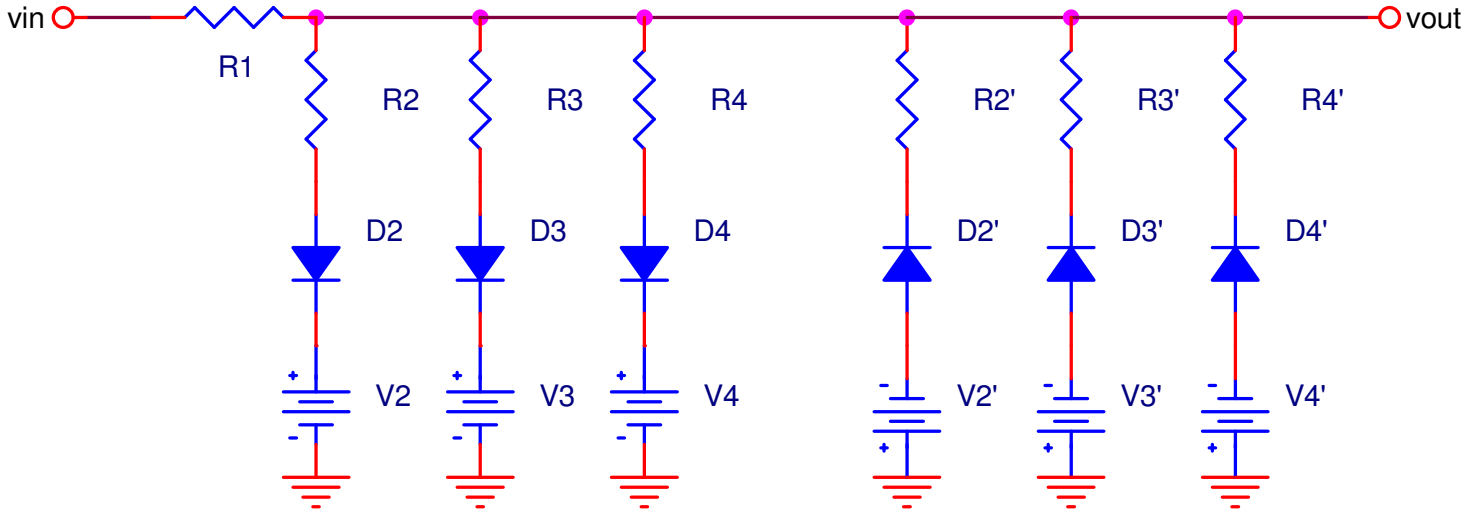
$$= \frac{2U_P C}{kR_A E}\left(2R_B + R\right) = ct$$

$$\eta = \frac{T_a}{T} = \frac{\left(R_B + \alpha R\right)}{\left(2R_B + R\right)} \sim \alpha$$



Low-medium frequency function generators

- **sine shaper circuit**



$v_{IN}=v_T(\theta)=V_T \cdot \theta/90^{o}= V_T \cdot 4t/T$ (V_T= triangle waveform amplitude)

$v_S(\theta)=V_s \sin\theta$ (V_S= sine amplitude)

$v_{out}(\theta)$ output signal approximates $v_S(\theta)$ using 4 segments/quadrant

Can obtain THD < 2%

Low-medium frequency function generators

- **sine shaper circuit**

Θ2=30º

Θ3=55º

Θ4=75º

Slope comp. $m_1 ... m_4$

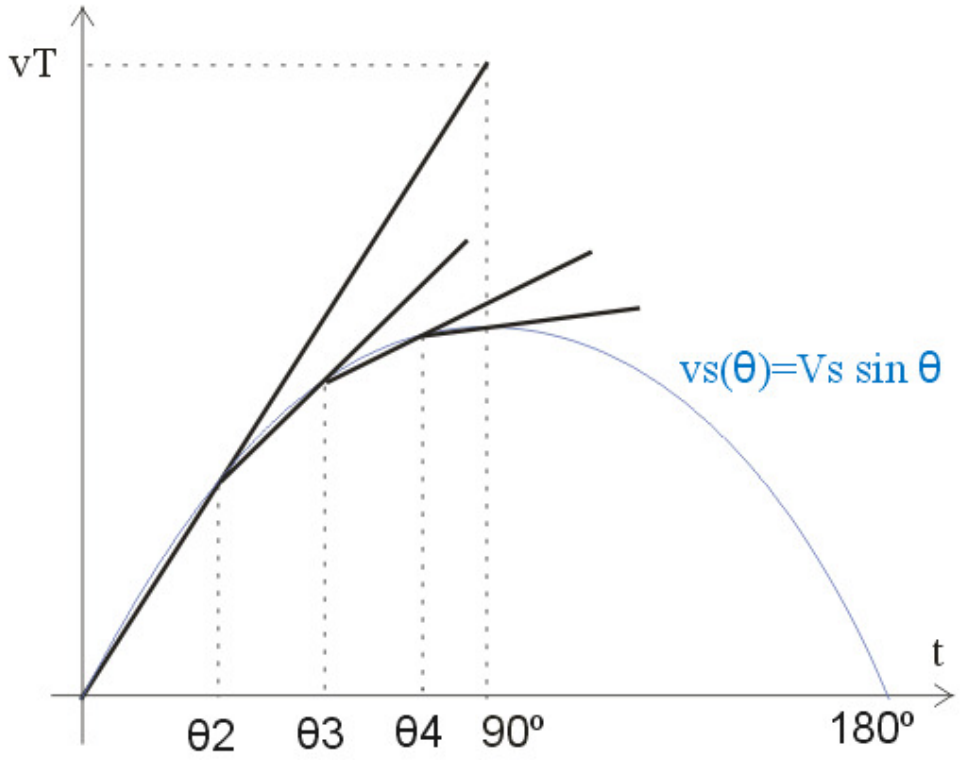
Comp. R_i from m_i values

$$m_1 = \frac{\theta}{90}$$

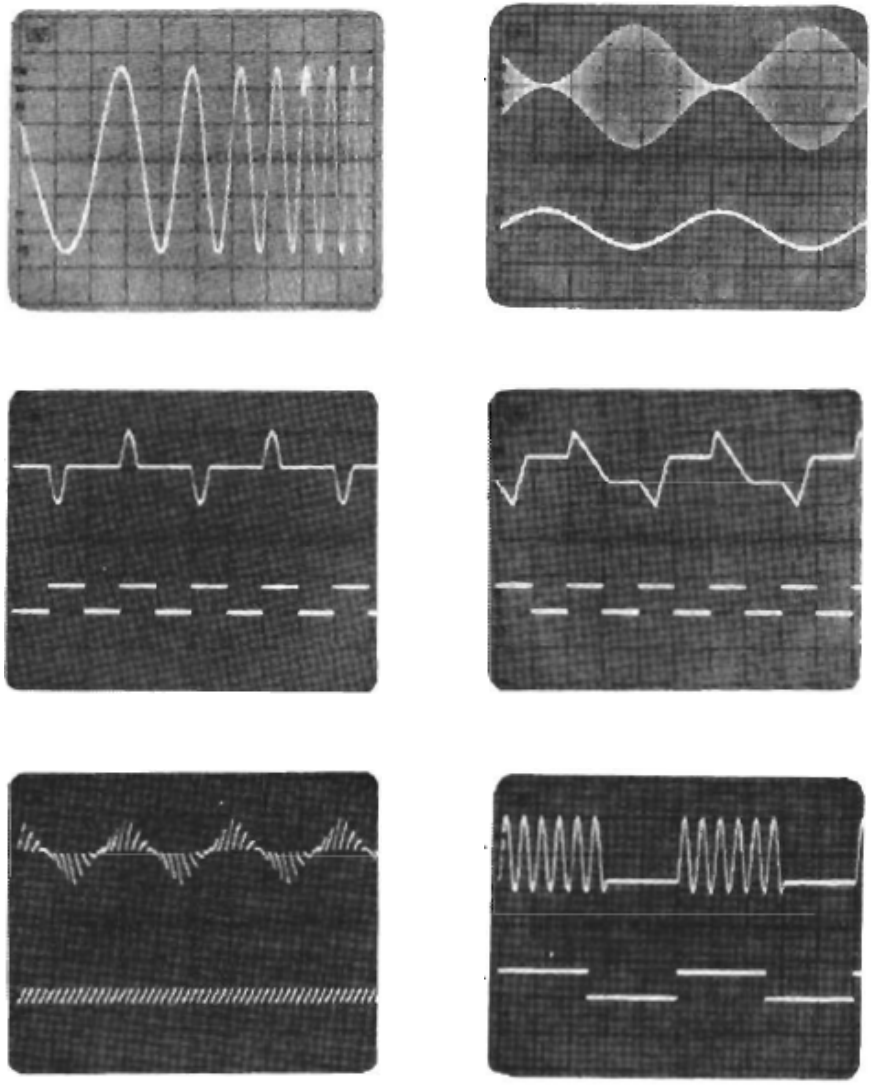
$$m_2 = \frac{R_2}{R+R_2}\frac{\theta}{90} = \frac{R_2}{R_1+R_2} m_1 < m_1$$

$$m_3 = \frac{R_2 \| R_3}{R+R_2 \| R_3} m_1$$

$$m_4 = \frac{R_2 \| R_3 \| R_4}{R+R_2 \| R_3 \| R_4} m_1$$

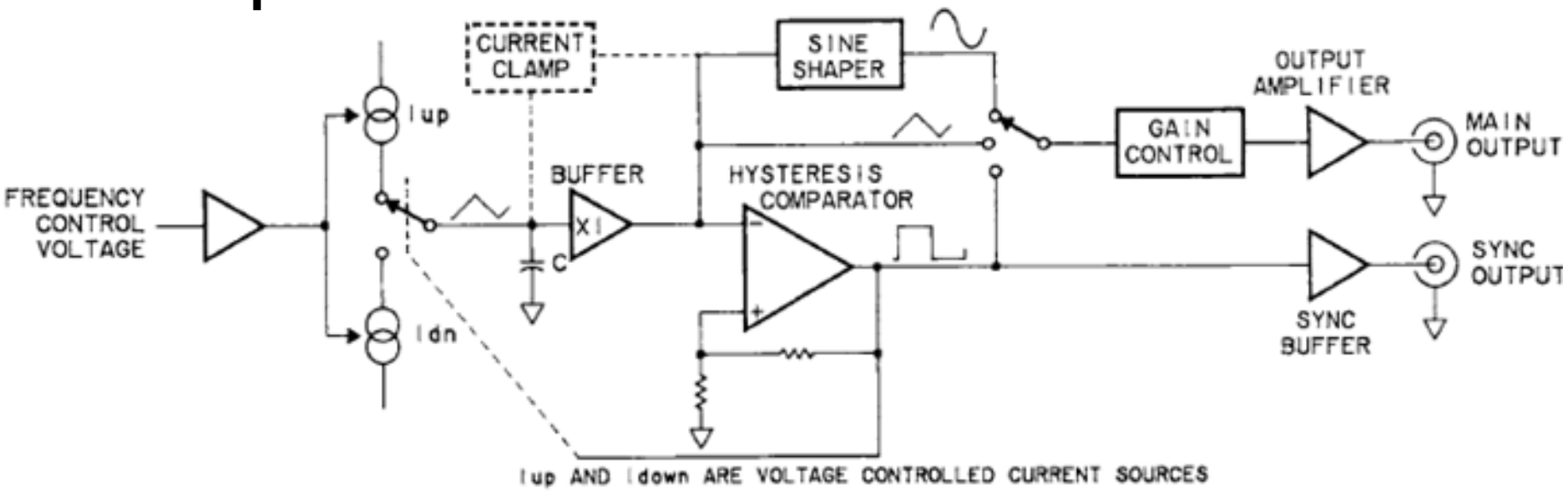


- **Example:** HP3314A



- Freq. range 0.001Hz – 19.99MHz
- Digital adjustment of amplitude, frequency, offset, symmetry, phase
- AM, FM, modulation with external signal
- External trigger
- GATE mode
- Standard waveform + ARB (arbitrary)

- **Example:** HP3314A – block scheme

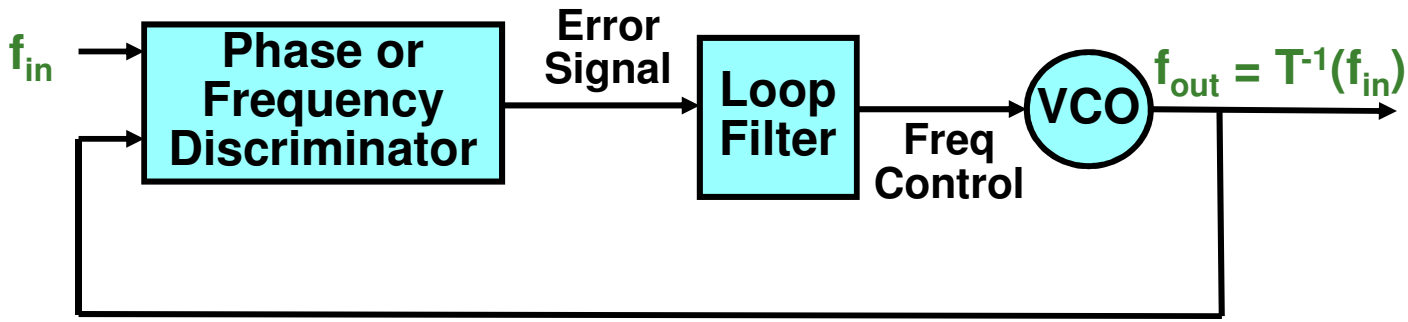


scale	Frequency range	C=	Buffer x1 / x10	Iup/Idn x 10
1	0.001-2Hz	2.77uF	x10	da
2	1Hz-20Hz	2.77uF	x10	nu
3	10Hz-200Hz	2.77uF	x1	nu
4	100Hz-2KHz	277nF	x1	nu
5	1-20KHz	27.7nF	x1	nu
6	10-200KHz	2777pF	x1	nu
7	0.1-2MHz	277pF	x1	nu
8	1MHz-19.99MHz	27.7pF	x1	nu

Phase Loop Lock (PLL)

Negative feedback control system where f_{out} tracks f_{in} and rising edges of input signal align to rising edges of output signal;

- PLL types:
  - analog (linear) PLL;
  - digital PLL;
  - all digital PLL;



Analog PLL

Loop classification

Loop Order (1st, 2nd, etc.)

Phase vs Frequency Lock

PLL Lower Near in Phase Noise

PLL: Loop Noise Converted to White Phase Noise

FLL: Loop Noise Converted to White Frequency Noise

FLL Settles Faster

Implementation

Analog Loops

Analog Phase Discriminator

Digital Phase Discriminator

Digital Loop (Filter)

Phase/Frequency Error Quantization

Continuous (or Near Continuous)

Bang-Bang (Sign of Error)

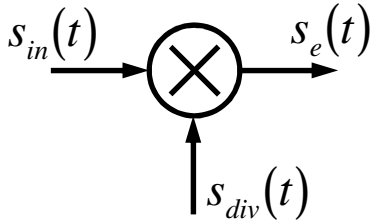
Analog PLL principle

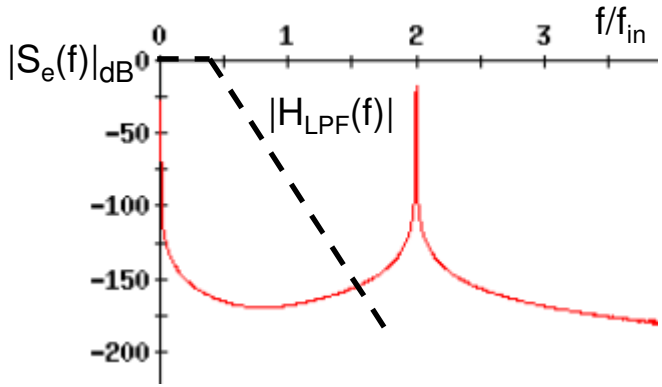
- Components:
  - Phase or frequency discriminator (PFD) – multiplier (analog inputs)
  - Loop filter
  - Voltage controlled oscillator (VCO)

- PFD

$$s_{in}(t)=A_1\sin(\omega_{in}t+\phi_{in})$$

$$s_{osc}(t)=A_2\cos(\omega_{in}t+\phi_{osc})$$





$$s_e(t)=s_{in}(t)s_{osc}(t)$$

$$=K_m\frac{A_1A_2}{2}\sin(\phi_{in}-\phi_{osc})+K_m\frac{A_1A_2}{2}\sin(2\omega_{in}t+\phi_{in}+\phi_{osc})$$

- Loop Filter – Low pass filter (LPF)

$$s_{contr}(t)=\mathcal{F}^{-1}\{H_{LPF}(f)\cdot S_e(f)\}=K_{LPF}K_m\frac{A_1A_2}{2}\sin(\phi_{in}-\phi_{osc})$$

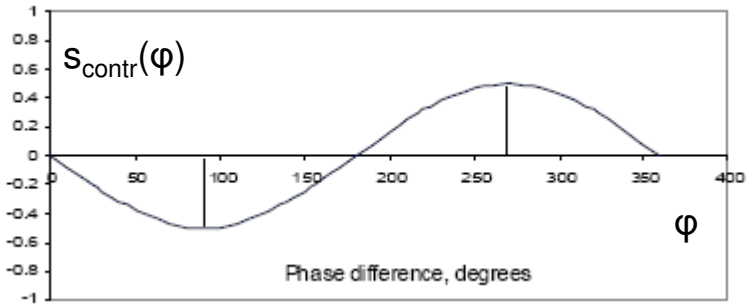
Analog PLL principle

• VCO – oscillator with output frequency controlled by input voltage

$$f_{osc} = f_0 + K_O \cdot s_{contr}(t)$$

$$\phi_{osc}(t) = 2\pi \int_0^t \left(f_{osc}(\tau) - f_0 \right) \mathrm{d}\tau$$

$$= 2\pi K_O \cdot \int_0^t s_{contr}(\tau)\,\mathrm{d}\tau = 2\pi K_O\, t \cdot s_{contr}(t)$$



$$s_{contr}(t) = K_{LPF} K_m \frac{A_1 A_2}{2} \sin\left(\phi_{in} - 2\pi K_O\, t \cdot s_{contr}(t) \right)$$

The equation of $s_{contr}(t)$ can be linearlized by making following assumption

For small θ, θ≈sin(θ)

$$s_{contr}(t) \approx K_{LPF} K_m \frac{A_1 A_2}{2} \left(\phi_{in}(t) - 2\pi K_O\, t \cdot s_{contr}(t) \right)$$

Analog PLL principle

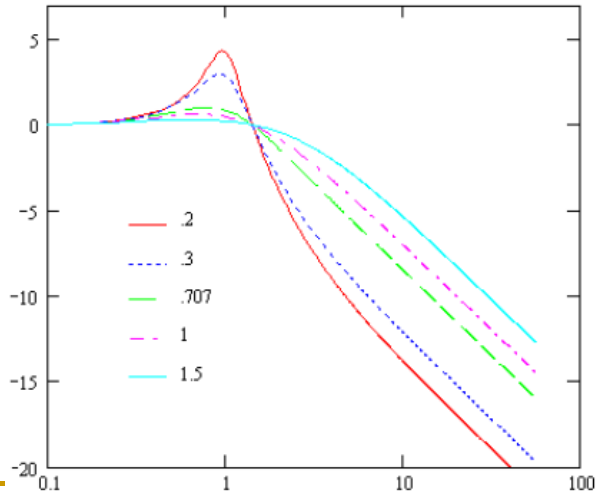
- Transfer function $H_{PLL}(s)$
  - K_m – gain of PFD;
  - K_{LPF}- gain of loop filter (LPF);
  - K_0 – gain of VCO;

$$s_{out}(t)=A_0\cos\left(2\pi f_0 t+K_0\int_{t_1}^{t_2}s_{contr}(t)\,\mathrm{d}\tau\right)$$

$$H(s)=\frac{P_f(s)}{1-P_f(s)P_b(s)}\qquad \left.\begin{array}{l}P_f(s)=\frac{1}{s}K_m K_{LPF}K_0 H_{LPF}(s)\\ P_b(s)=1\end{array}\right\}\Rightarrow H_{PLL}(s)=\frac{K\cdot H_{LPF}(s)}{s+K\cdot H_{LPF}(s)}$$

In case of $H_{LPF}(s)=\frac{1+s\tau_1}{1+s\tau_2}\Rightarrow H_{PLL}(s)=\frac{K(1+s\tau_1)}{\tau_2 s^2+K(1+s\tau_1)+K}$

$$H_{PLL}(s)=\frac{\omega_n^2+2s\xi\omega_n}{s^2+2s\xi\omega_n+\omega_n^2}\quad;\omega_n=\sqrt{\frac{K}{\tau_1}}\quad;\text{ damp factor }\xi=\frac{\omega_n\tau_2}{2}$$



Digital Phase Loop Lock (PLL)

- **PLL can acts as:**

Operation Inverter

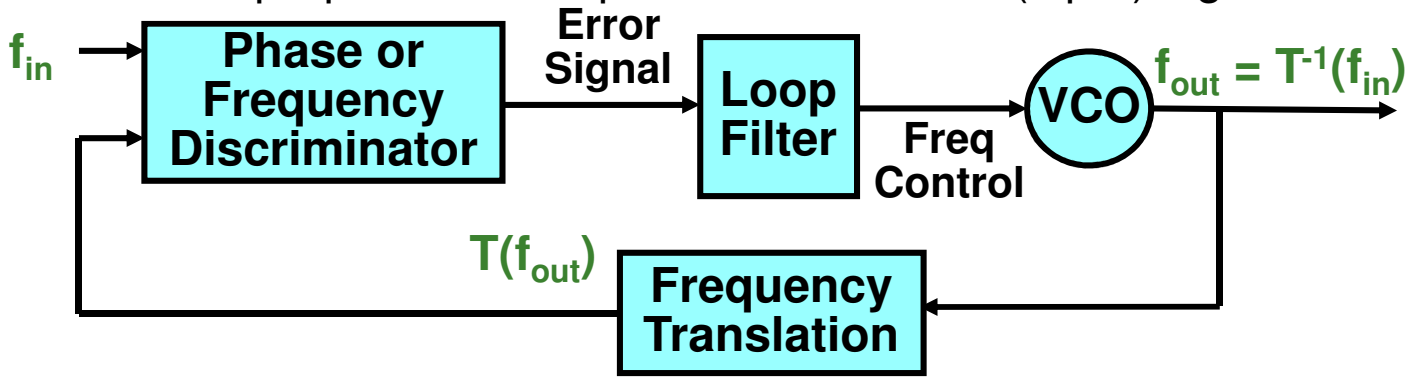
VCO output f_{out} goes through frequency translation $T(f_{out})$

Phase or Frequency Discriminator compares f_{in} to $T(f_{out})$ and generates error signal

Through Loop Filter and VCO frequency control, error signal driven to 0 so $f_{in} = T(f_{out})$; thus VCO output is inverse of T $f_{out} = T\text{-}1(f_{in})$

Tracking Filter

Uses bandwidth properties of loop to filter reference (input) signal



Digital PLL

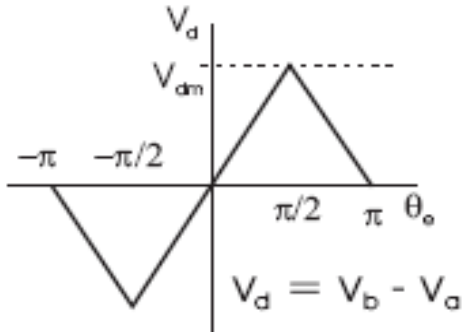
Digital Phase Loop Lock (PLL)

- **Digital PD**

Inputs – digital signals

Function interval φ [-π/2, +π/2]

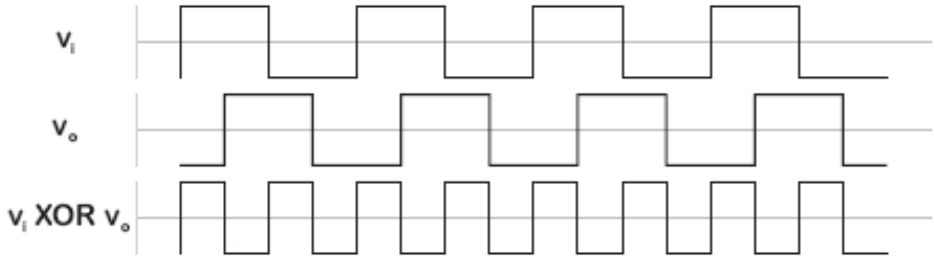
Functioning condition $f_{in} \approx f_{osc}$

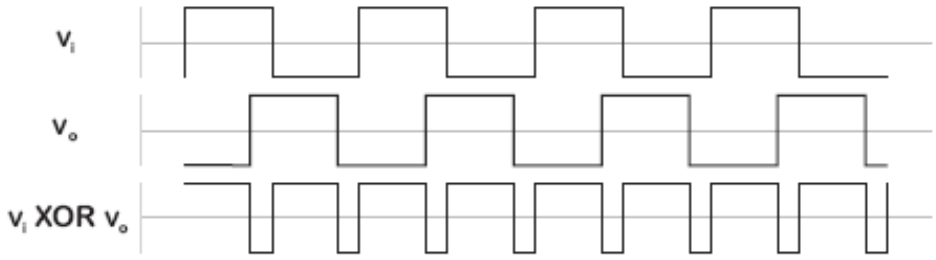


LPF selects DC component of XOR

$$V_d = V_a - V_b$$

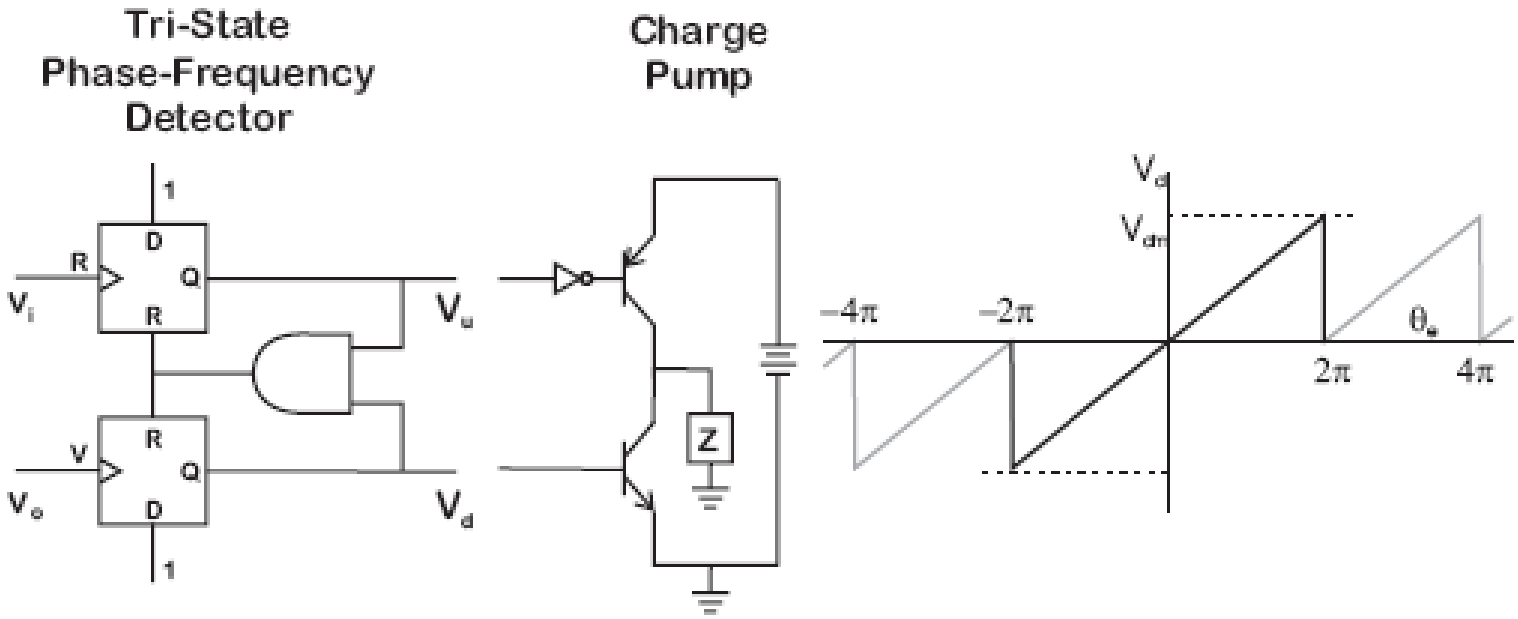
$$\begin{cases} V_d = \min \Rightarrow \Delta\phi = 0 \quad (V_a \text{ and } V_b \text{ in phase}) \\ V_d = 0 \Rightarrow \Delta\phi = \pi/2 \quad (V_a \text{ and } V_b \text{ in quadrature}) \\ V_d = \max \Rightarrow \Delta\phi = \pi \quad (V_a \text{ and } V_b \text{ in anti-phase}) \end{cases}$$





Digital Phase Loop Lock (PLL)

- **Digital PFD**

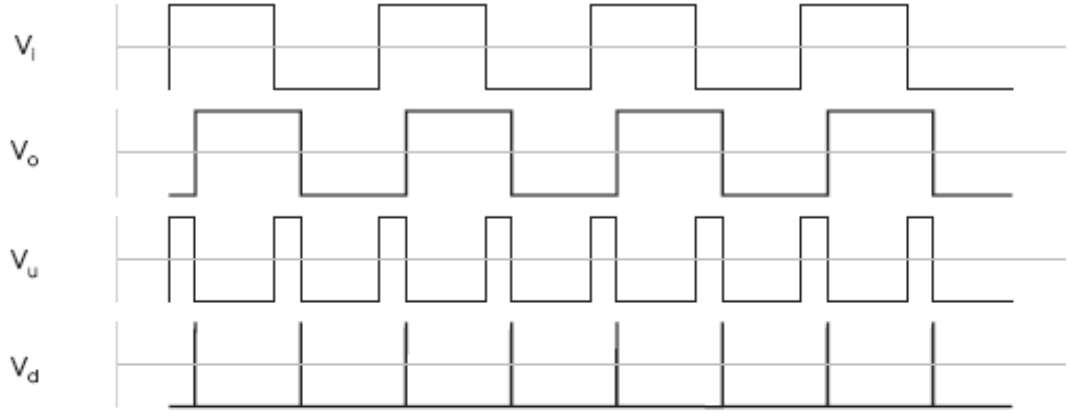


PFD = Phase-Frequency Discriminator

- Tracking phase range -2π... 2π (even $f_{in} \neq f_{out}$)
- V_U = UP (increase f_{osc} from VCO output)
- V_D= DOWN (decrease f_{osc})
- Z = LPF input and then command to VCO

Digital PFD

- **waveform for** $f_{in} = f_{out}$ and $\varphi_{in} \neq \varphi_{out}$

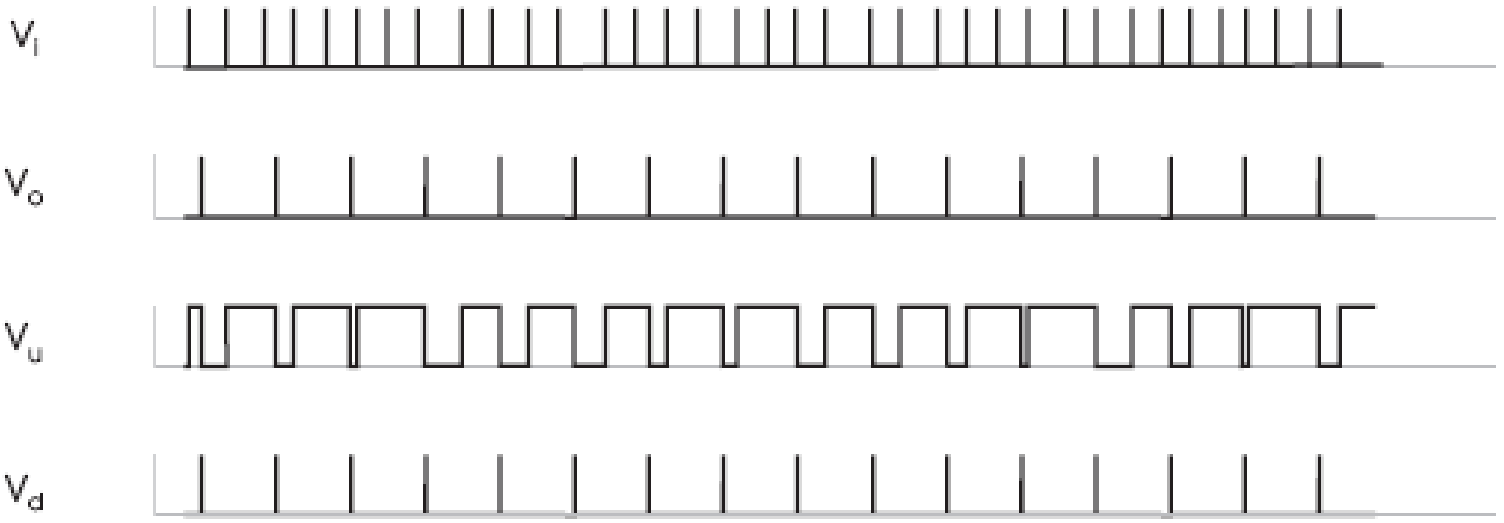


- First pulse (active rising slope) sets corresponding D flip-flop (exp. $V_i \rightarrow V_u$ on)
- Second pulse sets the other D flip-flop (exp. $V_o \rightarrow V_d$ on)
- AND gate resets both D flip-flop: V_u , V_d off (on time of V_d neglected)
- Case V_{out} slower than V_{in} ; V_{in} sets the first D flip-flop, $V_u > V_d \rightarrow$ "UP" ,

VCO will be "accelerated" and V_{out} will "catch up" V_{in}

Digital PFD

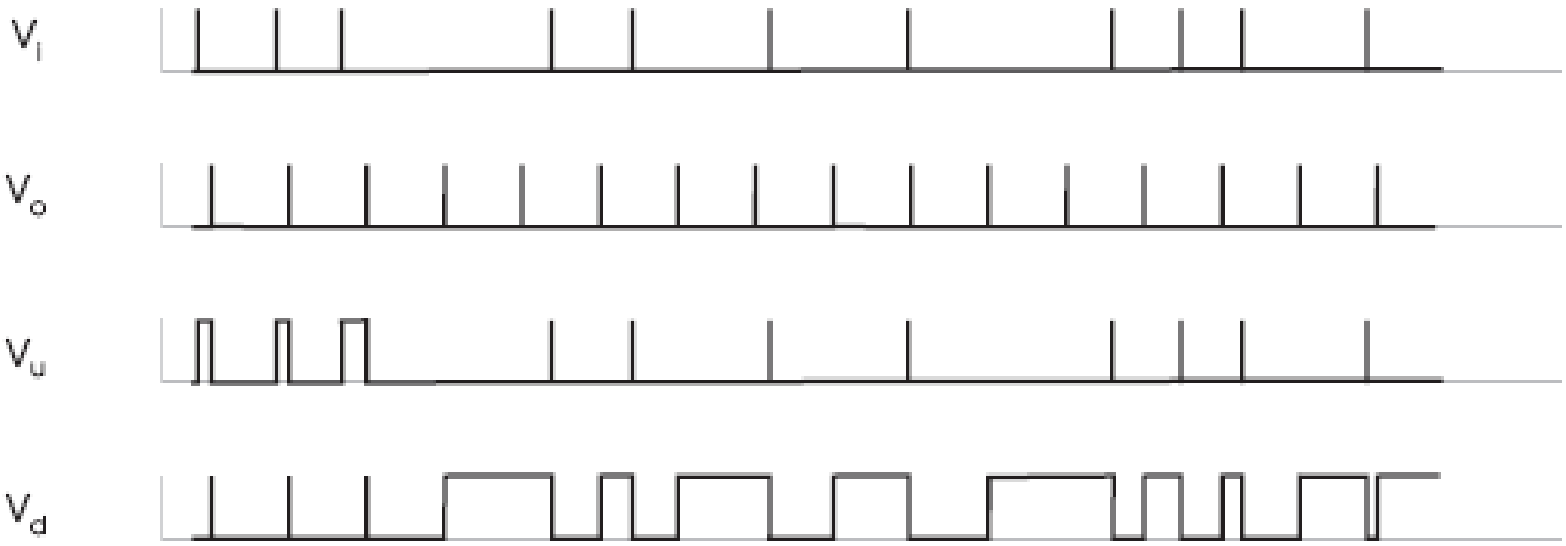
- **waveform for** $f_{in} \neq f_{out}$



- $f_{in} > f_{out}$, $V_u > V_d \rightarrow$ “UP” ,
- VCO will be “accelerated” and V_{out} will “catch-up” V_{in}

Digital PFD

- **waveform for** $f_{in} \neq f_{out}$ and *a periodic* signals



- Mean of f_{in} < mean of f_{out} , $V_u < V_d \rightarrow$ "DOWN" ,
- VCO will be "slowed down" and V_{in} will "catch-up" V_{out}

Digital Phase Loop Lock (PLL)

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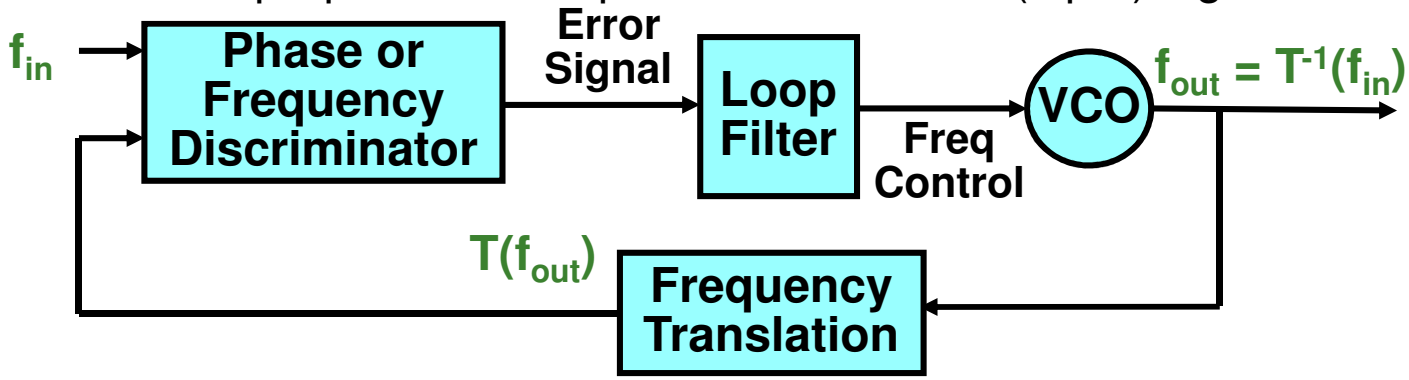

Digital PLL

Digital Phase Loop Lock (PLL)

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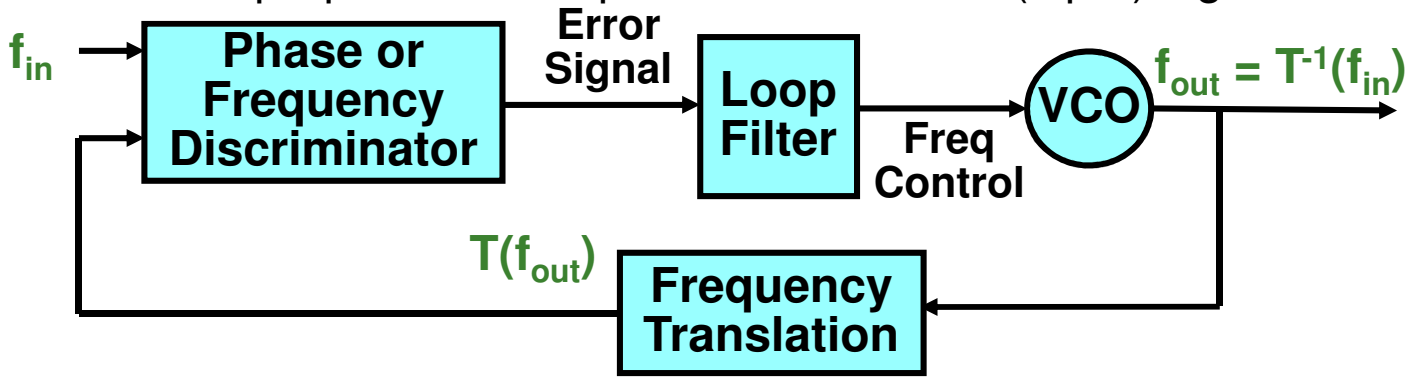

Digital PLL

Direct Digital Synthesizer (DDS)

• a technique that uses digital data processing to generate a frequency/phase-tunable output signal referenced to a fixed-frequency precision clock source

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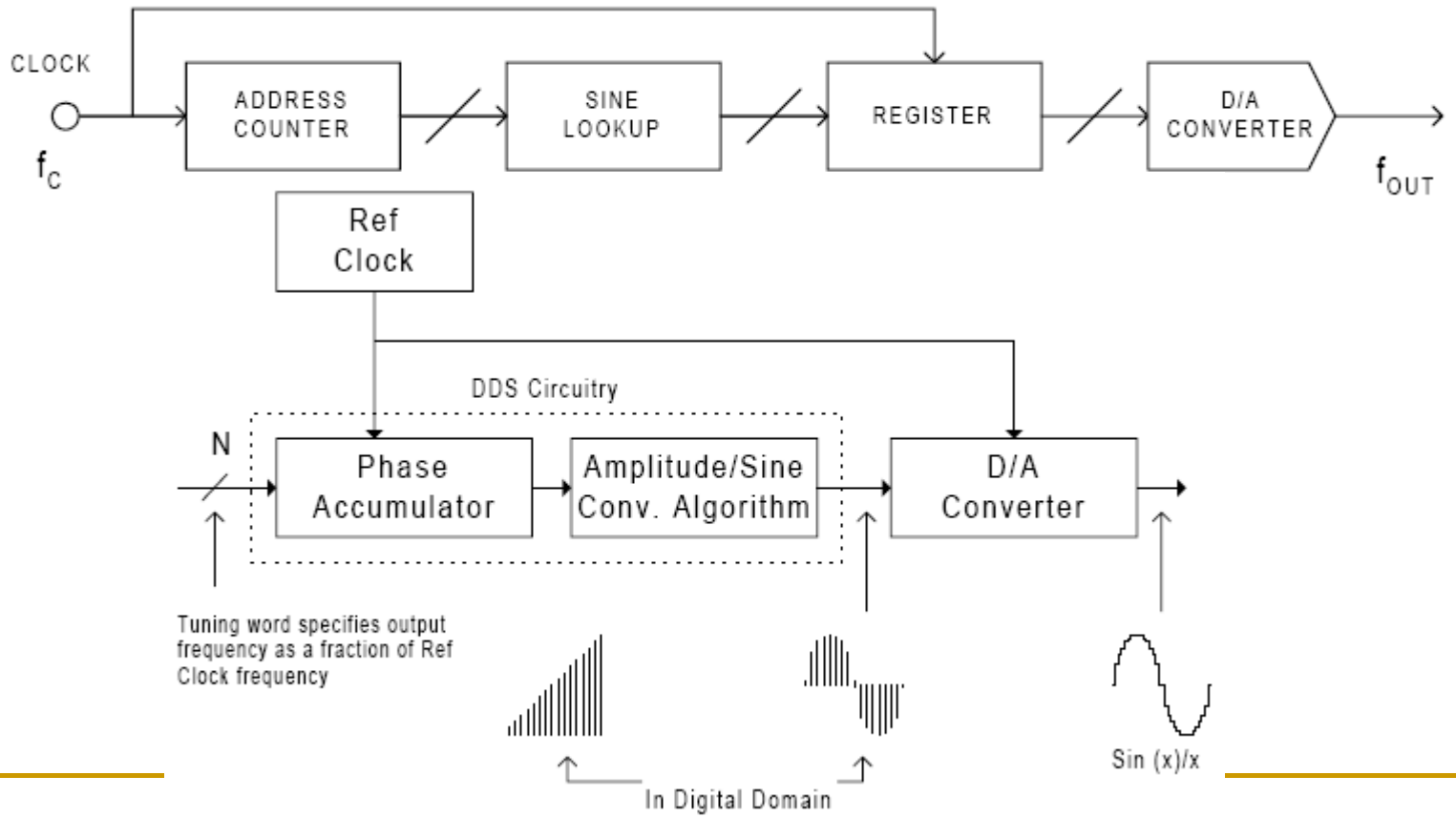

Direct Digital Synthesizer (DDS)

• a technique that uses digital data processing to generate a frequency/phase-tunable output signal referenced to a fixed-frequency precision clock source
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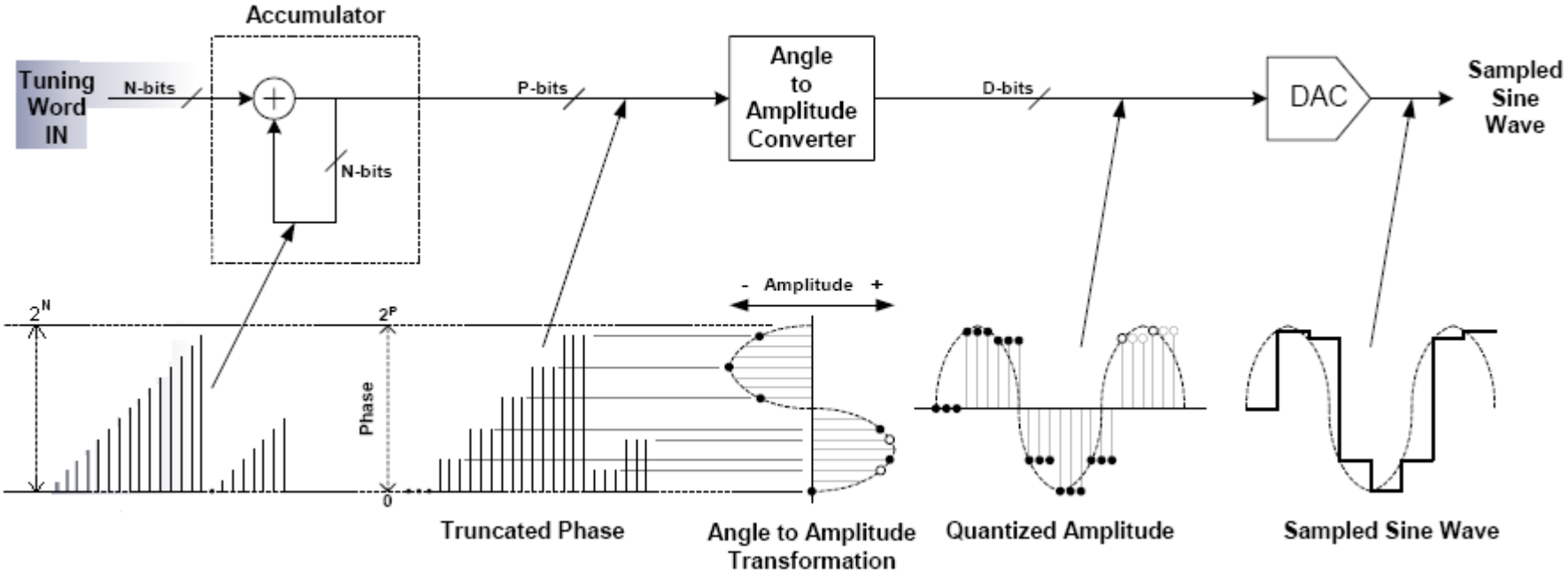
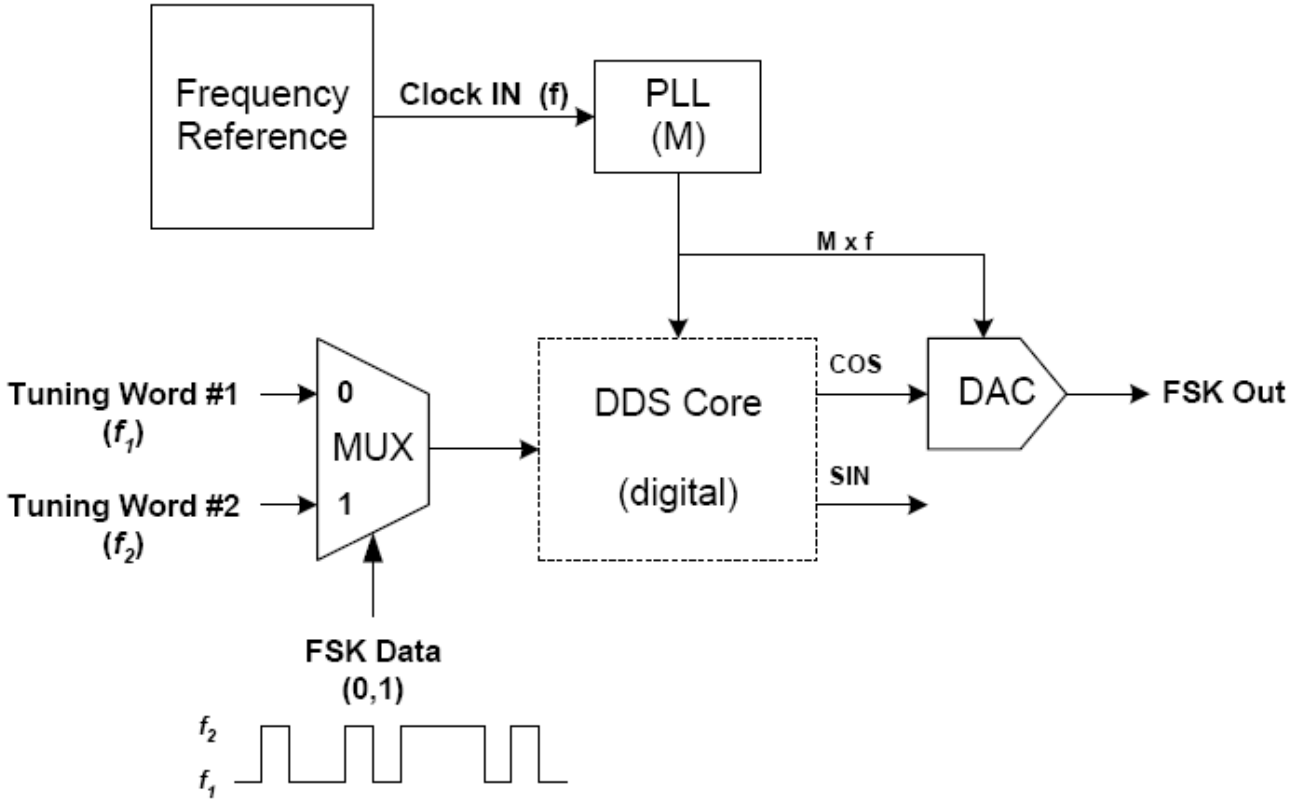


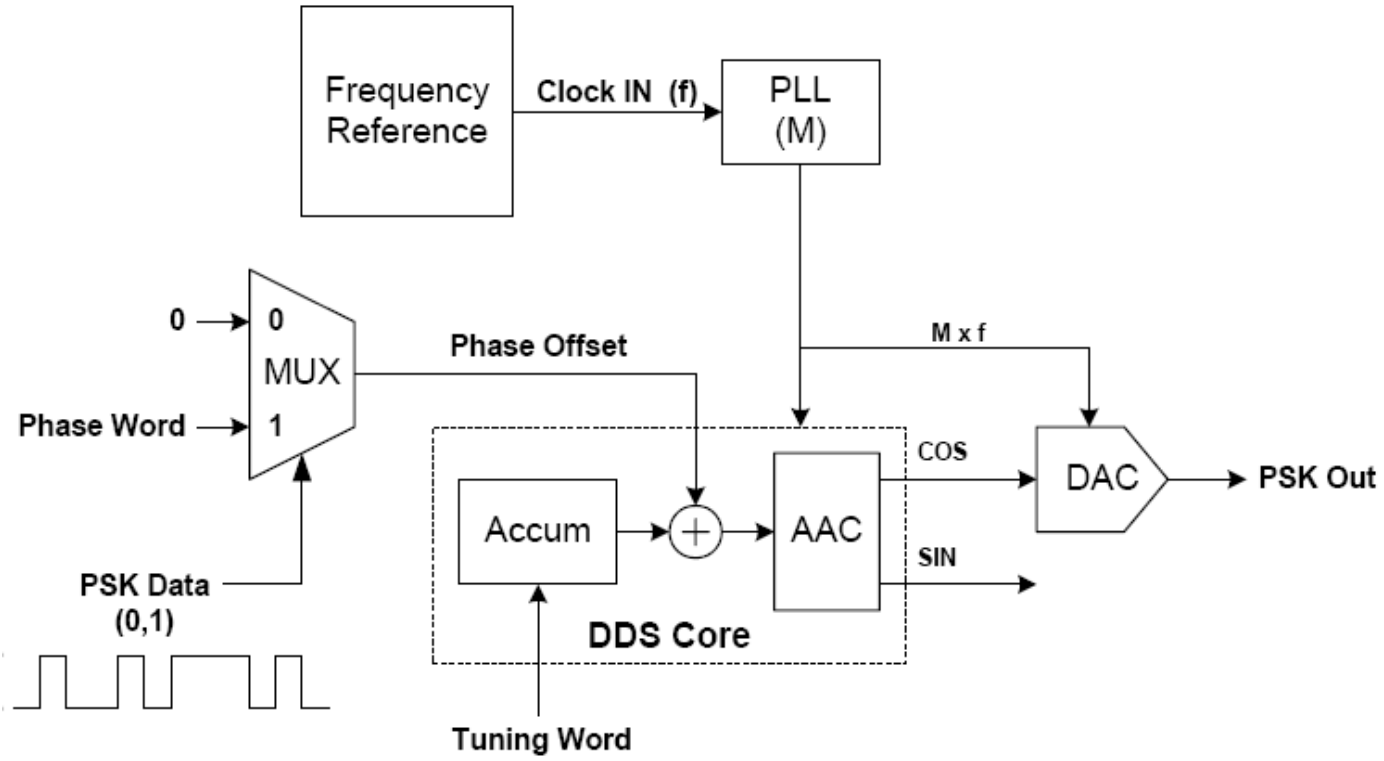
Direct Digital Synthesizer (DDS)

• Frequency Shift Keying



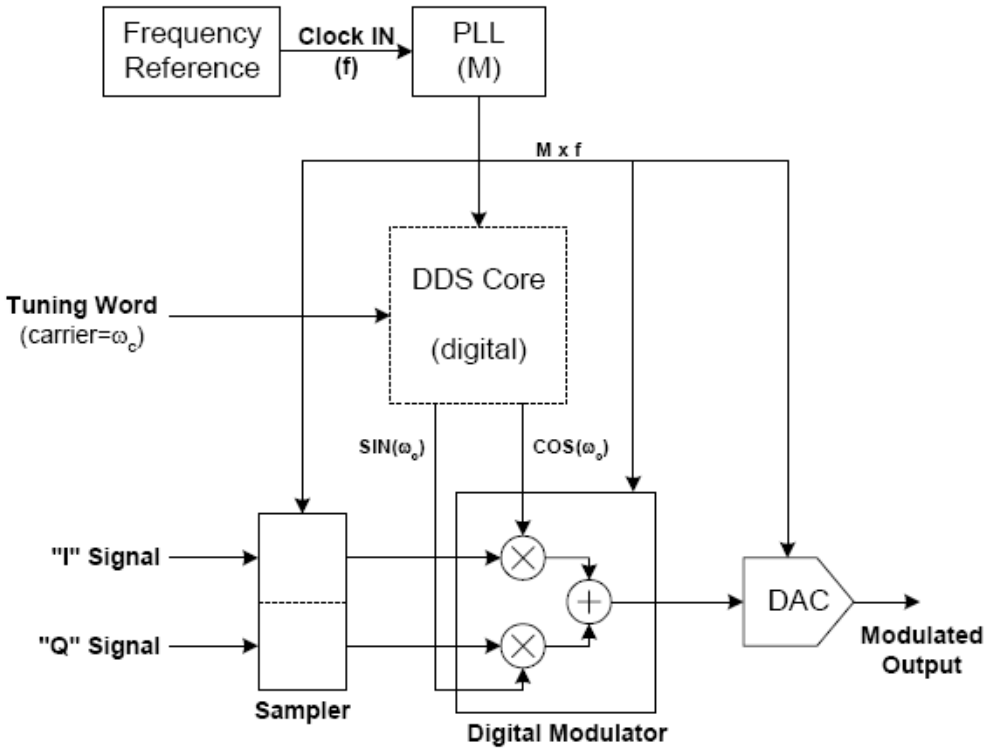
Direct Digital Synthesizer (DDS)

• Phase Shift Keying



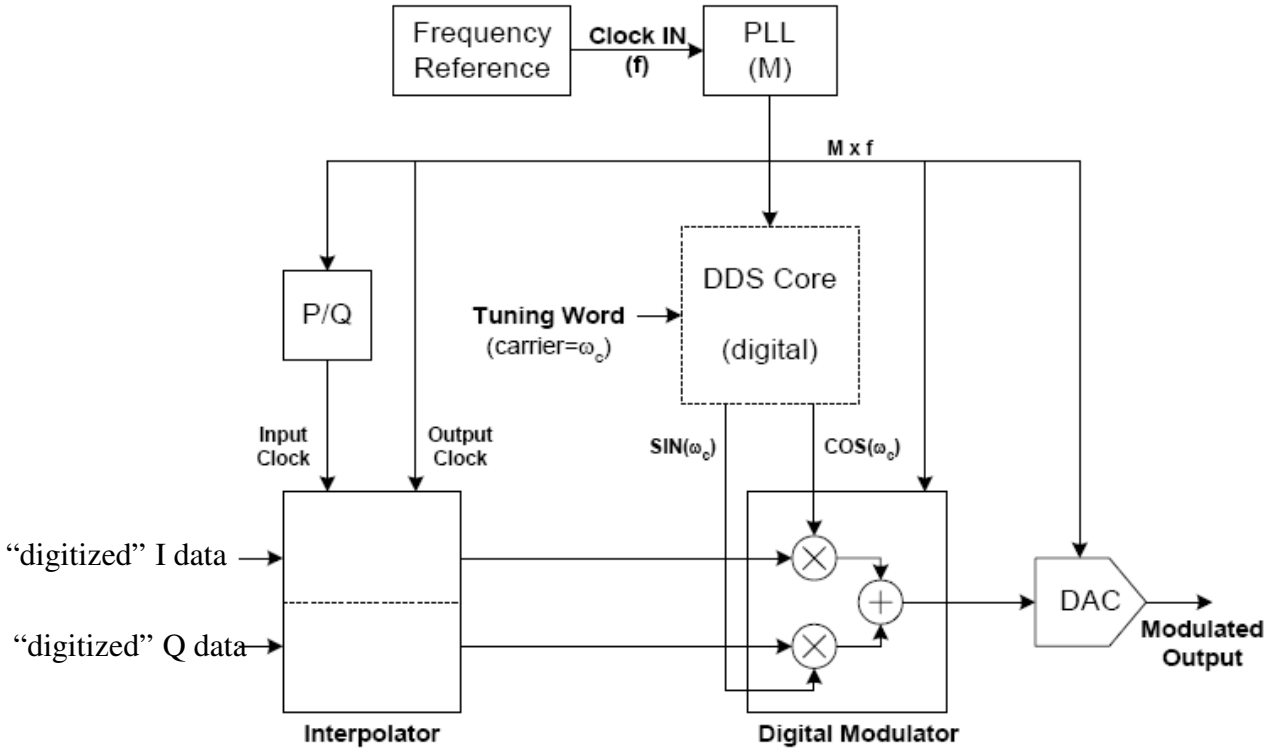
Direct Digital Synthesizer (DDS)

• Quadrature amplitude modulation



Direct Digital Synthesizer (DDS)

• Quadrature Up-Converter amplitude modulation



Direct Digital Synthesizer (DDS)

• Chirp modulation